A High Performance Controller for Parallel Operation of three-Phase UPSs Powering Unbalanced and Nonlinear Loads

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Abstract-- **In this paper, a high performance controller for parallel operation of uninterruptible power supplies (UPS) is proposed. The proposed controller is based on synchronous reference frame that is developed for parallel UPSs. Applying master-slave algorithm in this controller, power sharing and voltage regulation are controlled centrally by master UPS and commands are send through CAN bus to slave UPS. But each UPS performs voltage harmonic compensation locally and independently. Virtual impedance technique is used to share harmonic currents perfectly. Controller also is modified for unbalanced nonlinear loads. The performance of the proposed controller has been verified with simulation results for 20KVA, 380V three-phase parallel UPS.**

Keywords-component: Uninterruptible power supplies (UPS), Parallel operation, Synchronous reference frame controller (SRFC).

I. INTRODUCTION

With increasing sensitive and critical equipments, uninterruptible power supplies (UPSs) have become dramatically important. On other hand parallel operation of UPSs has considered because of its advantages such as expandability, modularity, maintainability, redundancy and reliability. Control system of parallel UPSs should supply three main requirements: 1) Regulation of load voltage with low THD. 2) Active and reactive power sharing. 3) Harmonic current sharing [1].

Various voltage regulation control approaches such as dead-beat controller, repetitive learning controller and synchronous reference frame controller (SRFC) have been proposed for three-phase UPSs [2-4]. In this paper SRFC controller is modified and developed for parallel operation of UPSs.

There are several methods for power and current sharing between parallel UPSs. These methods can be divided to two main parts: a) droop methods (or wireless method), b) active current sharing method (or communication based method). Droop method has higher reliability and do not require communication. However it has several drawbacks such as slow transient response, frequency and amplitude deviations, unbalance harmonic current sharing, and high dependency on the inverter output-impedance [5]. Therefore this method is suitable for distributed power supplies.

Active current sharing method can be classified as master-slave current-sharing scheme, average current-sharing scheme, maximum current-sharing scheme, and circular-chain current-sharing scheme [6-9]. In all these methods the current is regulated at computation period for fast dynamic response respect to load changes.

In active current sharing methods, harmonic current sharing can also be implemented. However, it needs high-speed data bus which increases cost of system. As a remedy, wireless methods can be used for harmonic current sharing. These methods include frequency and time domain approaches. In frequency domain approaches, droop method is used for harmonic components [10]. In time domain approaches a virtual resistance for harmonic components is considered at the output of UPSs [11]. This virtual resistance causes harmonic current sharing automatically. While in [11], virtual resistance is used for single-phase inverters, in this paper it is used for three-phase inverters.

II. UPS CONFIGURATION

Fig. 1 shows configuration of UPS used in this paper. The UPS includes a DC bus, three phase voltage source inverter, LC filter and delta-wye isolation transformer. Inverter is assumed without neutral wire. The delta-wye isolation transformer creates the natural path for zero sequence currents. Current of transformer (I_f) and capacitor voltage (V_C) are used as feedback signals.

III. CONTROL OF A THREE-PHASE UPS

Fig. 2 shows synchronous reference frame controller for three-phase UPS presented in [12]. The control system includes three parts: Positive sequence voltage controller (PVC), Negative sequence voltage compensator (NVC) and Harmonic voltage compensator (HVC). For balanced linear 3-phase load, PVC can perfectly track reference signal alone. The NVC compensates the negative voltage distortion due to

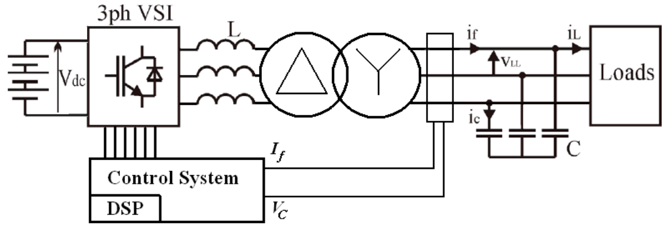

Figure 1. Configuration of UPS.

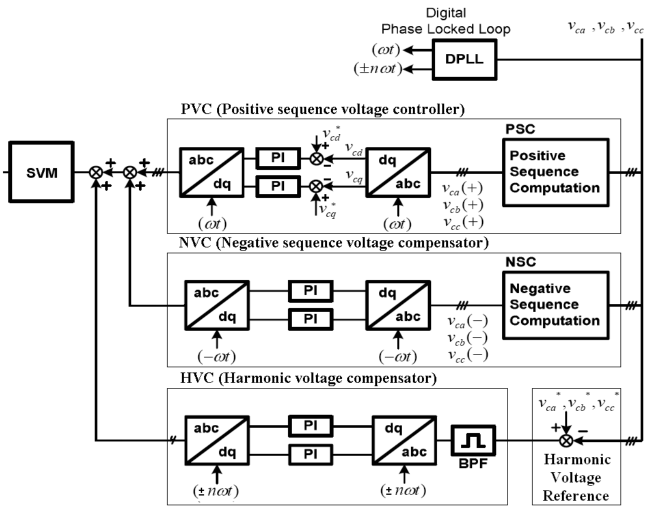

Figure 2. Synchronous reference frame controller for three-phase UPS.

unbalanced loads, and HVC compensates the harmonic voltage distortion due to non-linear loads.

Any unbalance output voltage can be expressed as three symmetrical components of positive, negative and zero sequences. Then the positive and negative components are obtained as:

$$\begin{bmatrix} v_{ca(+)} \\ v_{cb(+)} \\ v_{cc(+)} \end{bmatrix} = \frac{1}{6}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} + \frac{1}{j2\sqrt{3}}\begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} v_{ca(+)} \\ v_{cb(+)} \\ v_{cc(+)} \end{bmatrix} = \frac{1}{6}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} - \frac{1}{j2\sqrt{3}}\begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \quad (2)$$

where j is 90^o phase shift. While positive and negative components are controlled by PVC and NVC, the zero-sequence voltage current is forced to circulate ate the secondary winding of delta-wye transformer.

IV. MODIFIED PVC CONTROLLER

In this paper, the PVC controller has been modified for parallel operation of UPSs. Fig. 3 shows proposed PVC which has an internal current control loop to regulate the output current. Applying the current loop leads the controller to achieve a better dynamic response and also it is a key issue for parallel operation.

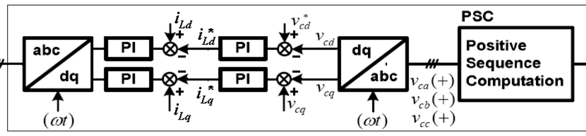

Figure 3. The proposed PVC controller.

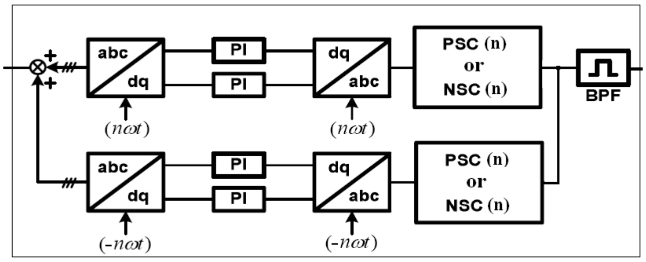

Figure 4. The proposed HVC compensator.

V. MODIFIED HVC COMPENSATOR

The symmetrical balanced harmonic component of the output voltage can be obtained by the dedicated bandpass filter whose characteristic frequency is corresponding to the selected harmonic frequency which should be compensated. These symmetrical balanced harmonic components can be transformed into DC signals by the Park transformation. Likewise PI controllers in HVC are operated with pure DC control quantities, and can provide the zero steady state errors for selected harmonic frequency. Sign + or – in ±nwt determine in respect to order of harmonic. For example the sign of 5th component is – and the sign of 5th component is +.

While the presented HVC in Fig. 2 is designed for detection of the symmetrical balanced harmonic component, this paper proposes a modified HVC for detection of unbalanced harmonic component (Fig. 4). In this method harmonic components are divided into positive and negative sequences. Equations (1) and (2) can be used for calculation of positive and negative sequences. Where j will be 90^o phase shift in relevant harmonic frequency. Upper and lower sequence computation blocks in Fig. 4 are selected regard to order of harmonic. For example for 3th and 7th harmonics, upper and lower blocks are PSC and NSC respectively, while for 5th harmonic, upper and lower blocks are NSC and PSC respectively.

VI. HARMONIC CURRENT SHARING

The Resistive output impedance can be a good candidate to share linear and nonlinear loads for parallel uninterruptible power supplies. Resistive output impedance for high-order current harmonics is obtained by subtracting a voltage which is proportional to the current harmonics from the output-voltage reference. Thus, the proposed output voltage reference can be expressed as:

$$v_{refh} = v_{ref}^{*} - \sum_{\substack{h=3 \\ odd}}^{11} R_h i_{fh} \quad (3)$$

The modified blocks which obtain the harmonic voltage reference for harmonic current sharing are shown in the Fig. 5.

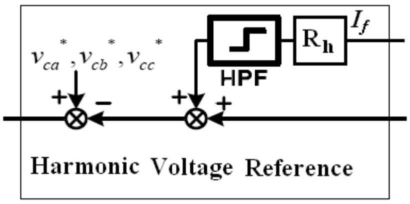

Figure 5. Harmonic voltage reference for harmonic current sharing.

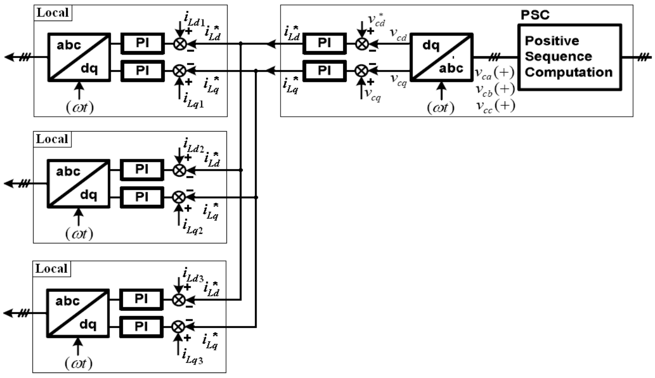

Figure 6. The Proposed PVC for parallel operation.

VII. PARALLEL UPSS CONTROL ALGORITHM

Master-slave current sharing method is used for parallel operation of UPSs in this paper. In this method, the control system is divided to two parts: Central and Local controller. Regarding to bandwidth limitation of data bus, all control system cannot be controlled centrally. So the NVC and HVC controllers can be controlled locally and PVC controller can be implemented both centrally and locally. Fig. 6 shows proposed PVC for parallel operation. Voltage control loop of PVC is implemented centrally in one of the UPSs called master UPS. This loop generates current references for both UPSs and they are sent through data bus to other UPSs (slave UPSs) through communication bus (CAN bus). Current loop of PVC is implemented locally in each UPS.

VIII. PARALLEL OPERATION

Fig. 7 shows overall diagram block of proposed control system for UPSs. The block has two selective switches (*SA* and *SB*) that create various control paths for different states. For the master UPS, both switches *SA* and *SB* should be in position 1. For a slave UPS before parallel operation, *SA* and *SB* are in positions 1 and 2 respectively. After soft start and synchronization, a slave inverter can connect to the AC bus. In this state, *SA* should be in position 2.

IX. SIMULATION RESULTS

The proposed control strategy has been implemented with two 10-kVA UPSs as simulation. Table I shows the specifications of UPSs. Table II shows used control parameters. Three various tests are performed on the proposed system: A) Balanced nonlinear three-phase 7.5 KVA load (three-phase rectifier) B) Unbalanced nonlinear single-phase load (single-phase rectifier) C) Step load (single-phase rectifier to two single-phase rectifiers).

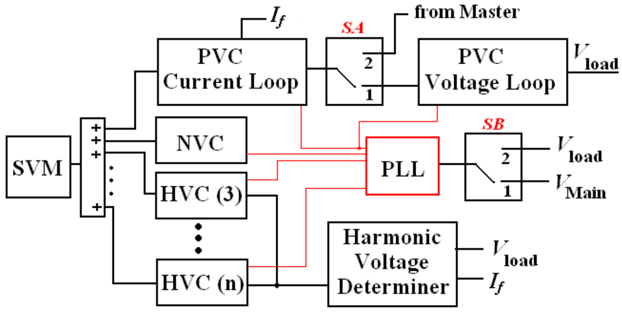

Figure 7. The overall diagram block of proposed control system.

TABLE I. SIMULATION PARAMETERS

Parameters	Values
V_{dc}	150 V
Transformer	(D11-Yg) 45/380 V
L_f	50 uH
R_f	0.01 Ohm
C_Y	38.6 uF
C_Δ	38.6 uF
Switchnig Frequency	3000 KHz
F_o	60 Hz
Sampling Frquency	15360 Hz

TABLE II. CONTROL PARAMETERS

Control Loop	**Kp**	**Ki**
Positive Voltage Loop	2	40
Negative Voltage Loop	-0.75	-40
Positive Current Loop	0.1	5
Positive & Negative Third Harmonic Loop	0.1	3
Positive & Negative Fifth Harmonic Loop	0.01	3
Positive & Negative Seventh Harmonic Loop	0.01	25

Figs 8-13 show results of test A. As shown in fig. 8, load voltage tracks main voltage very well. Balanced three-phase voltage of load can be seen in fig. 9. Harmonic components of load voltage are shown in Fig. 10 that satisfy industry standards [13]. Active and reactive powers are shared between two UPSs almost equally as shown in Fig. 11. Nonlinear load current is shown in Fig. 12. This current is shared between two UPSs as illustrated in Fig. 13.

Figs 14-19 show results of test B. As shown in these figures, voltage regulation, power sharing and harmonic current sharing is performed for unbalanced nonlinear load of test B.

Dynamic response of system is verified in test C. While a single-phase rectifier is connected to one of phase of UPSs, another single-phase rectifier connects to another phase. Figs 20-23 show results of the test. Load voltage maintains its synchronization with main voltage after connection of second rectifier (Fig. 20). Time and effective voltage of load is shown in Figs. 21 and 22. It can be seen that standard limits are satisfied. Finally Fig. 23 shows good power sharing between two UPSs.

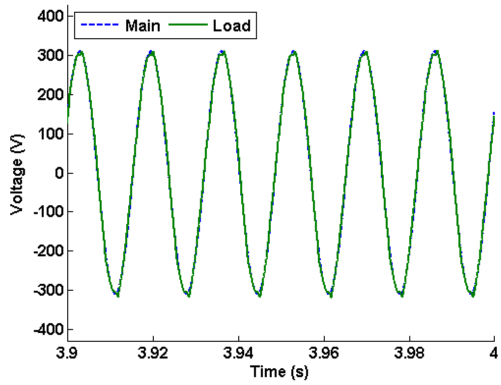

Figure 8. Phase voltage of main and load (Test A).

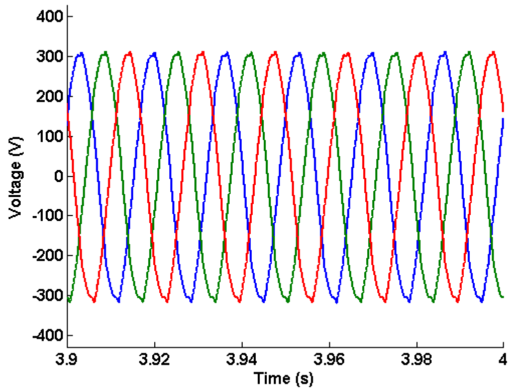

Figure 9. Phase voltage of load (Test A).

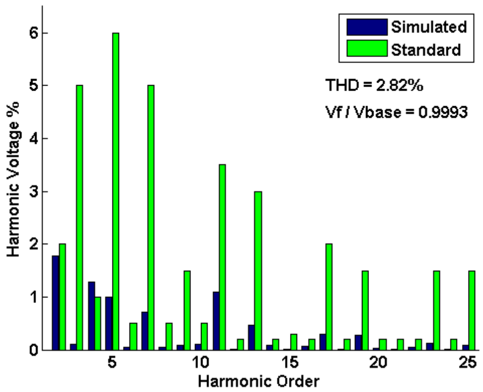

Figure 10. Spectra of load voltage (Test A).

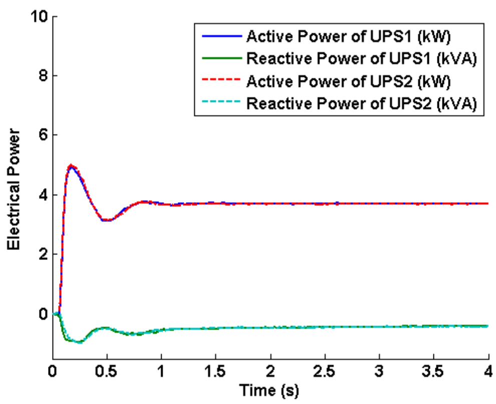

Figure 11. Active and reactive powers of UPSs (Test A).

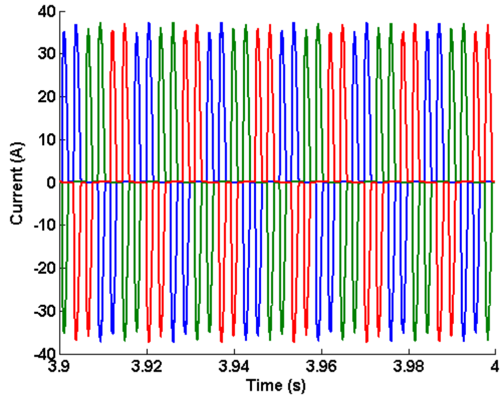

Figure 12. Load current (Test A).

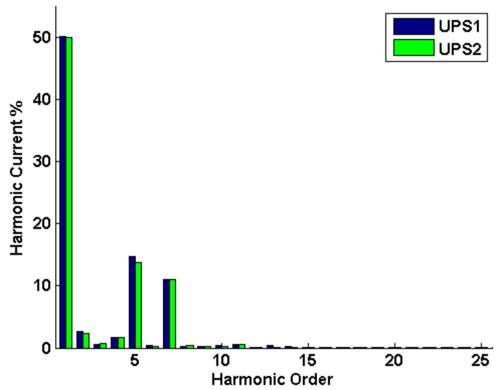

Figure 13. Harmonic current sharing (Test A.

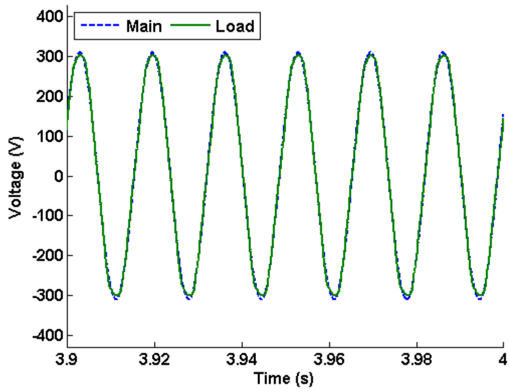

Figure 14. Phase voltage of main and load (Test B).

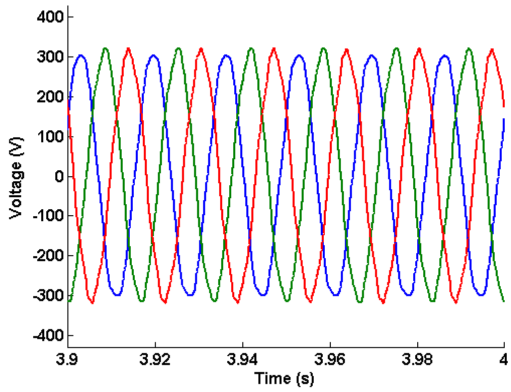

Figure 15. Phase voltage of load (Test B).

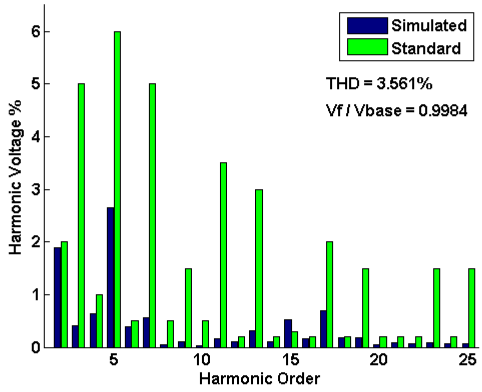

Figure 16. . Spectra of load voltage (Test B).

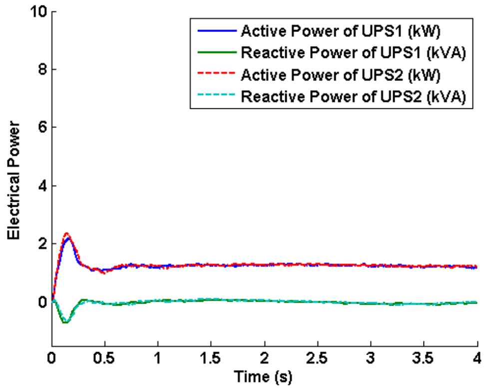

Figure 17. ctive and reactive powers of UPSs (Test B).

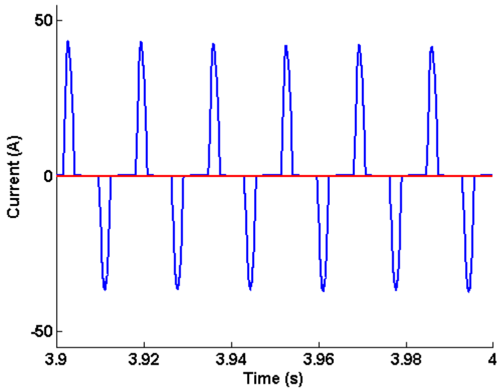

Figure 18. Load current (Test B).

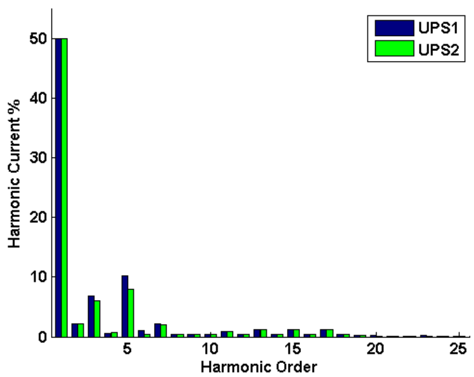

Figure 19. Harmonic current sharing (Test B).

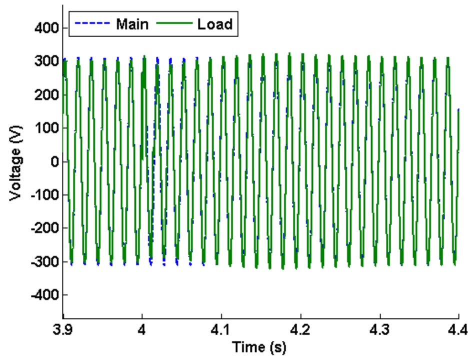

Figure 20. Phase voltage of main and load (Test C).

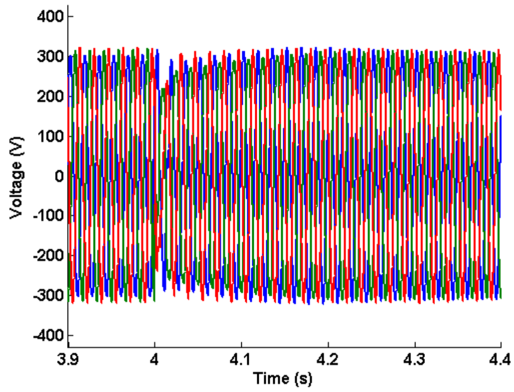

Figure 21. Phase voltage of load (Test C).

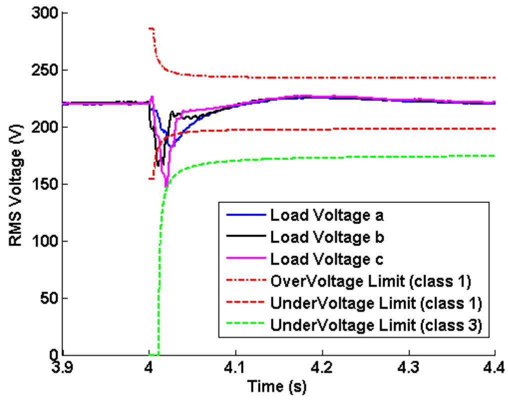

Figure 22. Effective voltage of load (Test C).

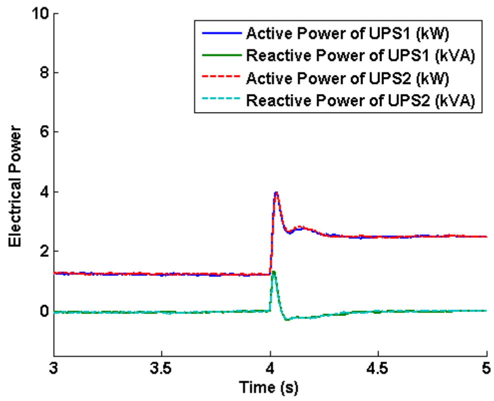

Figure 23. Active and reactive powers of UPSs (Test C).

X. CONCLUSIONS

In this paper, synchronous frame UPS control for nonlinear load was modified for parallel operation of two UPSs. In the proposed method, master-slave approach was adopted, in which a serial communication is employed between the UPSs. Fundamental voltage control and power sharing was implemented both with master and slave UPSs. Harmonic control was implemented locally. A resistive harmonic control was adopted for harmonic sharing. Simulation results verified the performance of the proposed controller.

XI. ACKNOWLEDGMENT

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