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Research Article

Deadbeat Control of a Modified Single-Phase Five-Level Photovoltaic Inverter with Reduced Number of Switches

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In this article, a modified single-phase five-level photovoltaic inverter is proposed with a single DC voltage source and six semiconductor switches. Compared with the presented inverters, the introduced topology has the advantage of decreased device count and the first switching frequency for high blocking voltage switches. The proposed PV inverter is implemented without clamping diodes and transformers, which leads to a decrement in size and, consequently, the weight of the converter. In addition, for the proposed topology, space vector pulse width modulation (SVPWM) is deployed that reduces the complexity of multilevel modulation. In order to obtain the optimal output voltage of the inverter, the deadbeat controller is suggested as a rapid dynamic, low-computation digital control method. This closed-loop inverter is implemented in TMS320f28335 digital signal controller to evaluate the performance of the proposed inverter under nonlinear and linear loads. Simulation and laboratory prototype results show that IEC 62040-3 harmonic constraints is met for the proposed photovoltaic inverter in standalone applications.

1. Introduction

Increased greenhouse gas emissions have led to the development of renewable energy. In recent years, a large number of zero fossil fuel energy buildings were built in the world that uses renewable energy as a source of whole energy. The use of off-grid photovoltaic inverters is preferred at loads that are located far away from the grid. By this method, there will be no need for transmission lines or it can also decrease the network congestion issue such as new transmission line costs. Under these conditions, a hybrid network, consisting of renewable distributed generation resources and the energy storage system, is designed to be responsive to load with high reliability. An inverter converts DC voltage of the photovoltaic system to sinusoidal voltage with constant amplitude and frequency. The inverter must be able to provide the desired voltage quality in a variety of single-phase linear or nonlinear loads. Multilevel inverters (MLI) have an appropriate harmonic spectrum. Currently, multilevel renewable energy inverters have presented to increase efficiency and reduce the space and weight of converters [1].

MLI have several advantages over conventional two-level inverters. Some of these advantages include generating the voltage with low harmonic distortion, reducing the dv/dt stress on the semiconductor switches, decreasing switch failure rate, increasing reliability, improving electromagnetic compatibility, and improving common-mode voltage. Besides these, the rated voltage of the switches is less, which reduces the cost of the inverter [2].

Less individual and total harmonic distortion in MLI reduces the LC filter size, which diminishes the converter's weight and transportation costs. Series switches in multilevel inverters increase conductive losses, but collector-emitter voltage is decreased which leads to the reduced inverter switching losses.

Therefore, increasing the efficiency of MLI reduces energy consumptions and reduces greenhouse gas emissions. On the

other hand, utilizing multilevel converters results in less THD and less switching frequency, which reduces switching losses. Therefore, MLI can use low-frequency semiconductors [3].

Different topologies are presented for the five-level inverters, for example, neutral point clamp (NPC), flying capacitor (FC), and cascaded H bridge (CHB) converters, which are known as traditional multilevel topologies [4].

Clamping diodes are required in NPC topology, and the blocking voltage on each power switch or diode is equal to a quarter of the total blocking voltage of five-level inverter. The principal advantage of the NPC inverter is the low switching frequency, while its weakness is the uneven distribution of thermal losses in semiconductors. This issue limits the switching frequency of this topology.

The active neutral point clamp (ANPC) inverter has been developed as a treatment for NPC problems in power loss distribution, and clamping diodes have been replaced with switches [5].

The FC converter has a modular structure. Each switch pair with a capacitor forms a power cell. These inverters have higher voltage levels than other converters, and their disadvantages are the large capacitors and the converter control complexity in balancing the capacitor voltage [6]. The CHB inverter has a rapid dynamic response; furthermore, in a symmetrical type, two or more single-phase H series inverters are connected, which reduces the repairing time and the overhaul costs. The CHB converter has a redundant switching state which increases the fault tolerance [7]. The voltage stress on each switch of this converter is equal to the DC voltage source voltage. The main disadvantage of this topology is its requirement of isolated DC voltage sources, which means more transformers are required. Therefore, in CHB inverters, costs and dimensions are increased [8].

MLI have some limitations such as the increased number of power electronic switch, which increases installation space, overall MLI cost, and complexity of the inverter system.

According to the above goals, the remainder of the paper is organized as follows. In Section 2, the structure and switching vectors of this single-phase five-level reduced device count inverter are introduced. In Section 3, the single-phase SVPWM is presented to be applied to the inverter. Also, the open-loop simulation results of the converter are discussed in this section, and the proposed converter is compared with the presented inverters. In Section 4, the proposed MLI and some of the presented structures are compared in terms of the number of parts such as the number of unidirectional and bidirectional switches, independent DC voltage sources, capacitors, and diode clamps. In Section 5, some predictive control methods are evaluated, and finally, the deadbeat controller is proposed. In Section 6, MATLAB simulations and laboratory prototype results are performed to investigate the performance of the converter under nonlinear and linear loads. Finally, the conclusion and the suggestion are given in Section 7.

2. Proposed Topology

The proposed single-phase MLI can be categorized as a combining with some change between full bridges and the active neutral point clamp MLI topology. The topology is represented in Figure 1. One semiconductor switch is connected to the middle of the DC link capacitors to create a five-level inverter. The switching states are classified in Table 1. With proper control, the DC voltage of two series capacitors can balance; therefore, this topology does not require two independent DC voltage sources. This converter is called the Γu5L inverter, due to the location of the switches.

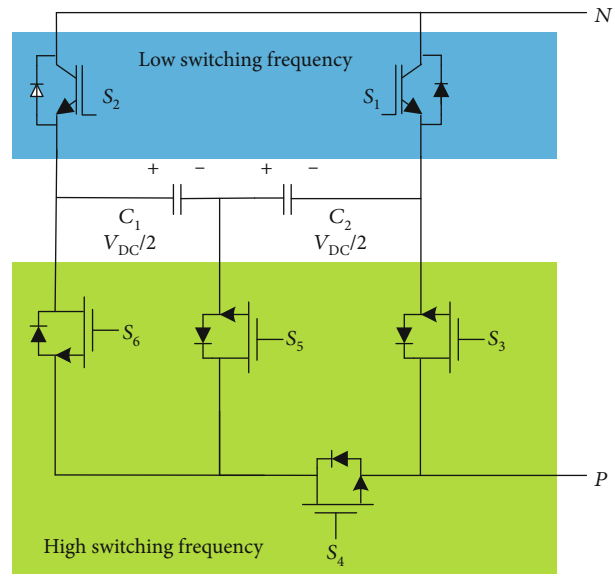


Figure 1: Proposed five-level inverter drawings.

Table 1: Proposed five-level inverter general switching vectors.

S_1	S_2	S_3	S_4	S_5	S_6	V_{out}	Vector	C_1	C_2
1	0	0	1	0	1	$-V_{DC}$	V_1	-	-
1	0	0	1	1	0	$-V_{DC}/2$	V_2	*	-
1	0	1	0	0[⊠]	0	0-	V_3	*	*
0	1	0	1	0	1	0+	V_4	*	*
0	1	0	1	1	0	$V_{DC}/2$	V_5	-	*
0	1	1	0	0[⊠]	0	V_{DC}	V_6	-	-

∗: no effect; -: discharging.

According to Table 1 except in the case of zero modes, at each level, maximum of three conducts and three changes occurred.

Table 1 is the general switching mode of the converter. But in the SVPWM method, when switching is happening between V_2 and V_3 in section C, there is chance of an intermediate unwanted switching state and same thing happens during the switching between V_6 and V_5 in section A. Therefore, the switching table in the SVPWM method is modified so that only two switches change position in each section. This is done by turning on the S_5[⊠] in V_3 and V_6 that do not affect the output voltage.

Figure 2 shows the inverter operation, including different switching vectors. V_1 and V_6 vectors discharge C_1 and C_2 capacitors. V_2 discharges C_2 capacitor. V_5 discharges C_1

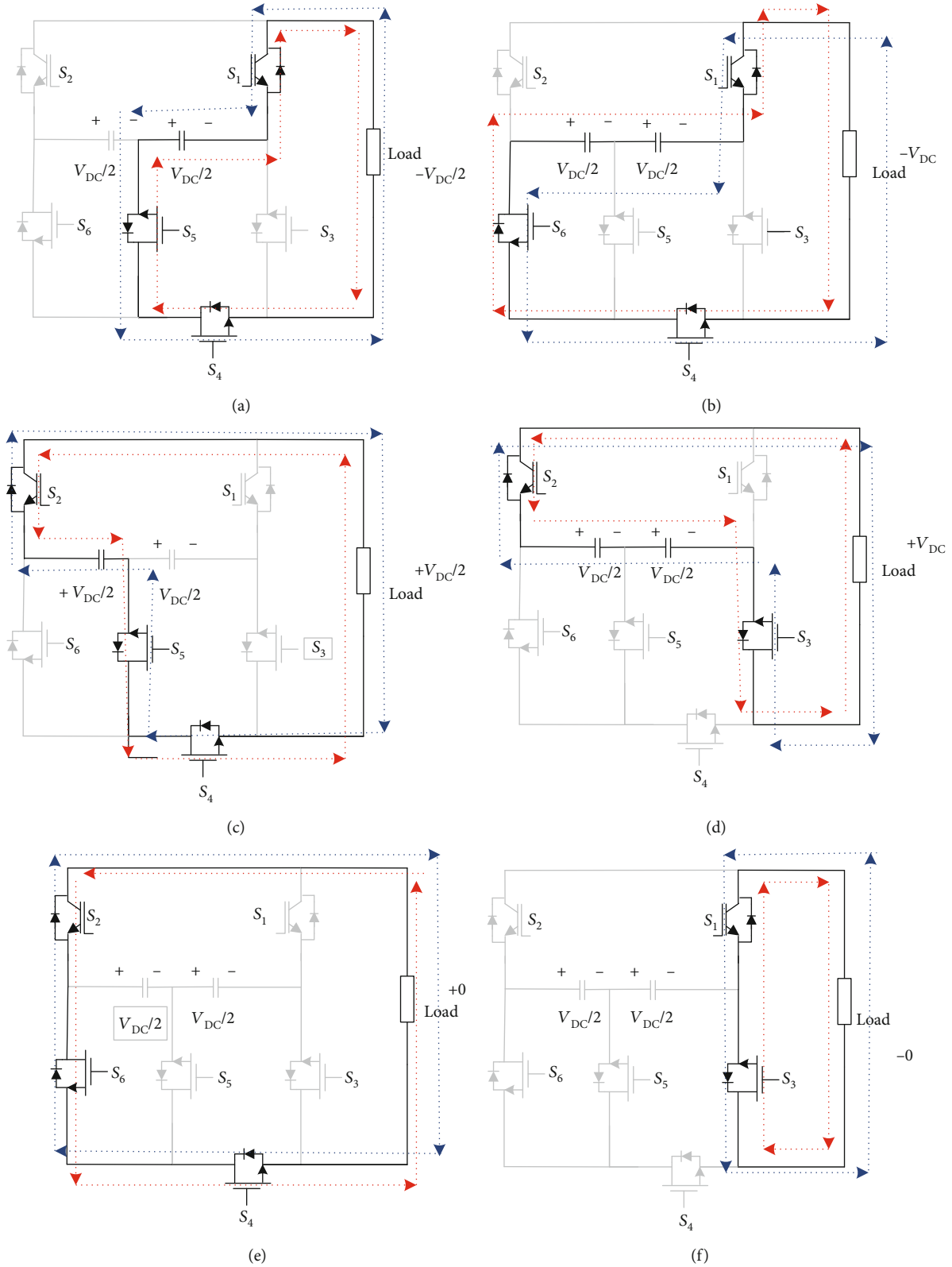


FIGURE 2: Ƭu inverter operation in the following vectors: (a) -V_{DC}/2. (b) -V_{DC}. (c) +V_{DC}/2. (d) +V_{DC}. (e) Positive zero voltage. (f) Negative zero voltage.

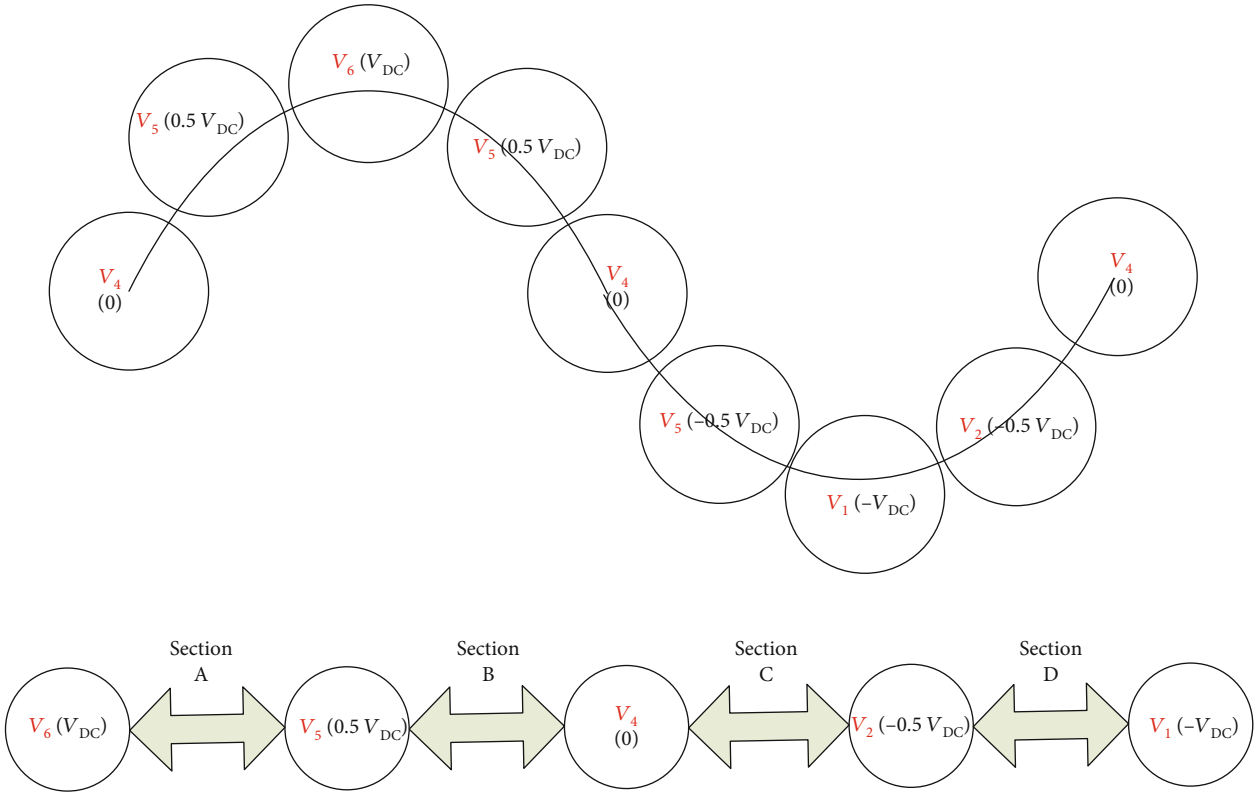


Figure 3: SVPWM switching mode of Γu inverter.

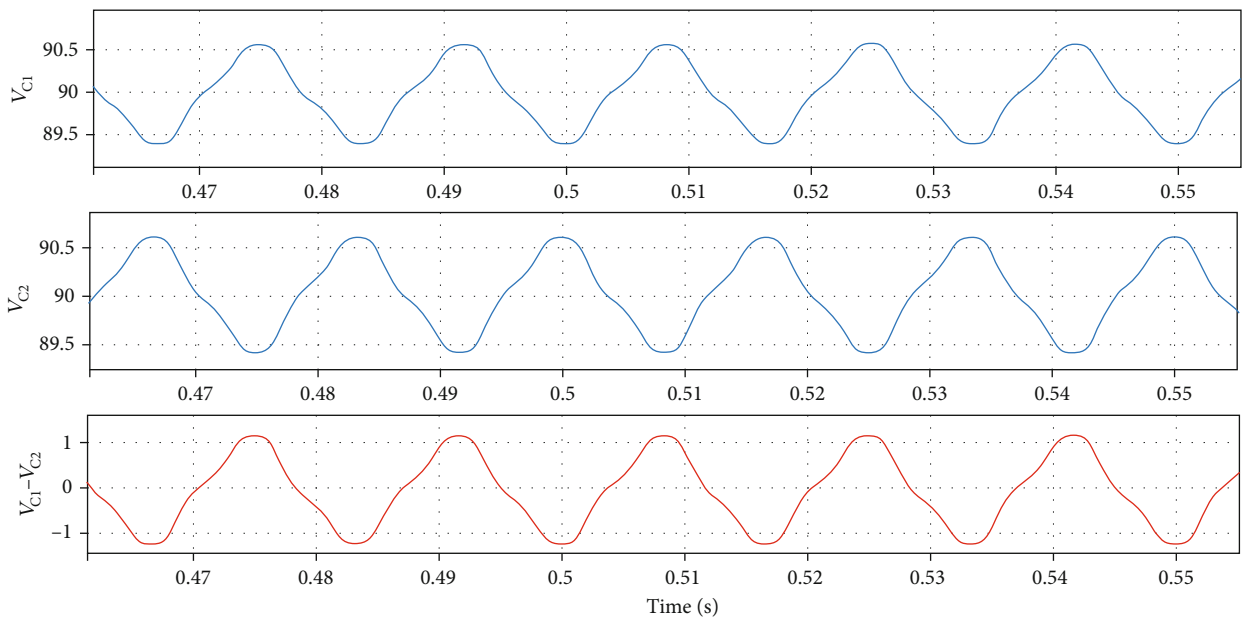


Figure 4: DC link capacitor voltage range without compensator.

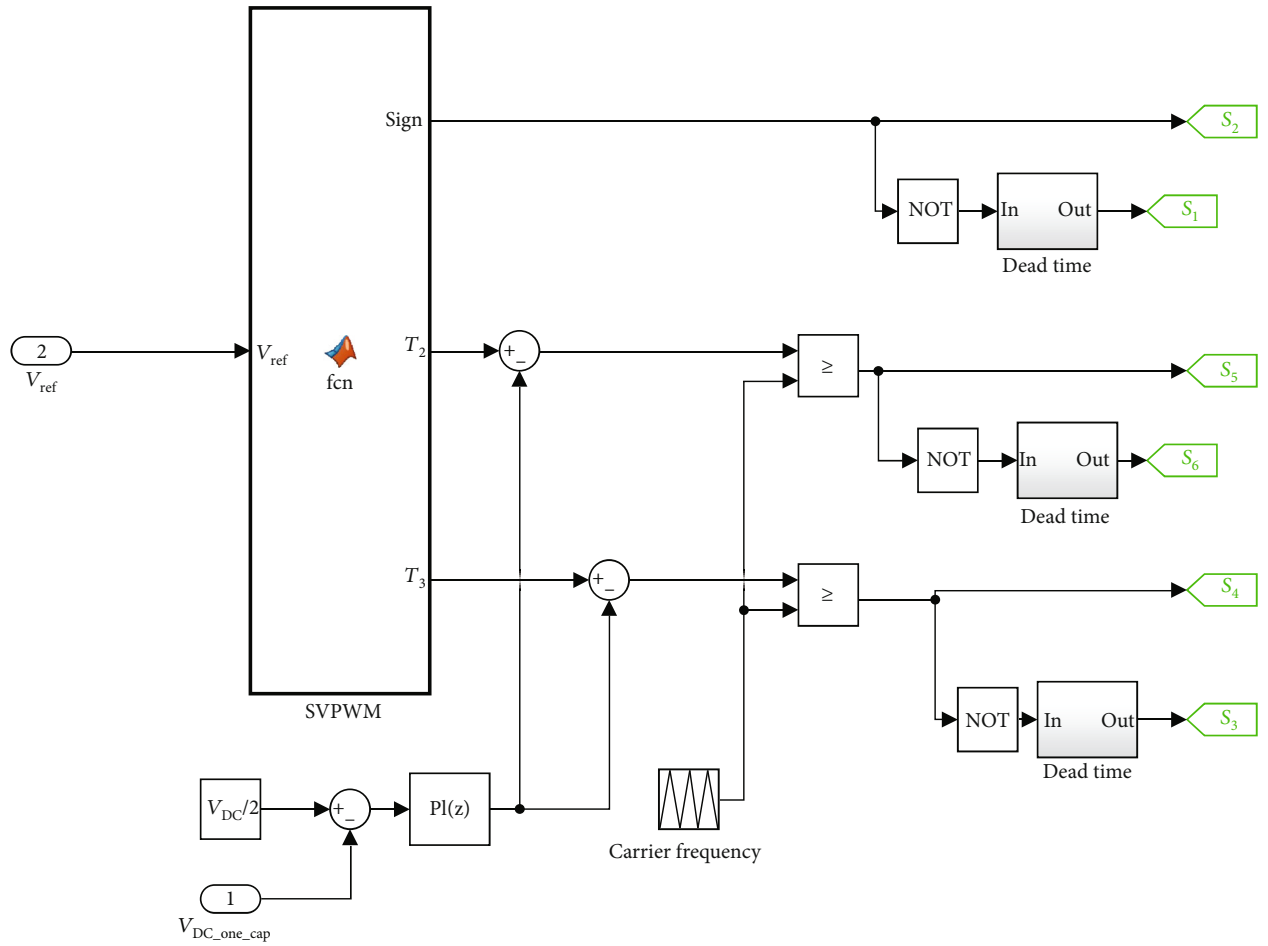


Figure 5: DC link capacitor voltage balancing control loop.

Table 2: Open- and closed-loop simulation parameters.

Parameters	
Carrier frequency	20 kHz
Frequency	60 Hz
Load resistance	80 Ω
DC link voltage	180 V
Filter inductance (L)	5 mH
Filter capacitors (C)	4.3 μF
Dead time	2 μs
DC link capacitors	2200 μF
Modulation index open-loop test	0.8642

capacitor. Zero voltage vectors are V_4 and V_3, and their application has no effect on the voltage of C_1 and C_2.

3. Modulation Method

Various two-level modulation methods have been entered into MLI. The PWM method is changed into phase shift (PS-PWM) and level shift (LS-PWM) techniques, and in any MLI has many impacts on the voltage balancing in capacitors and THD of the inverters [8].

The existence of several carrier waves in the MLI which has also the requirement to apply dead time to prevent short circuit has led to the need for FPGA, which increases the complexity of the converter design.

Few works have been published SVPWM algorithm for single-phase MLI, and this method is often used for three-phase inverters [9].

A single-phase five-level SVPWM technique is proposed for Γu5L inverter. This technique is recommended for ease of implementation of modulation in DSP and decreases the complexity in the switching time calculation [10].

Figure 3 illustrates the voltage vectors and four voltage sections determination in Γu5L inverter. Voltage and switching vectors have been shown in Table 1.

According to Equation (1), T is the modulation period. T_1 and T_2 are the duty cycles of the actuated voltage vectors in each section, respectively.

$$T = T_1 + T_2. \tag{1}$$

Solving these two unknown variables, T_1 and T_2 require another equation obtained from the following equations in each section.

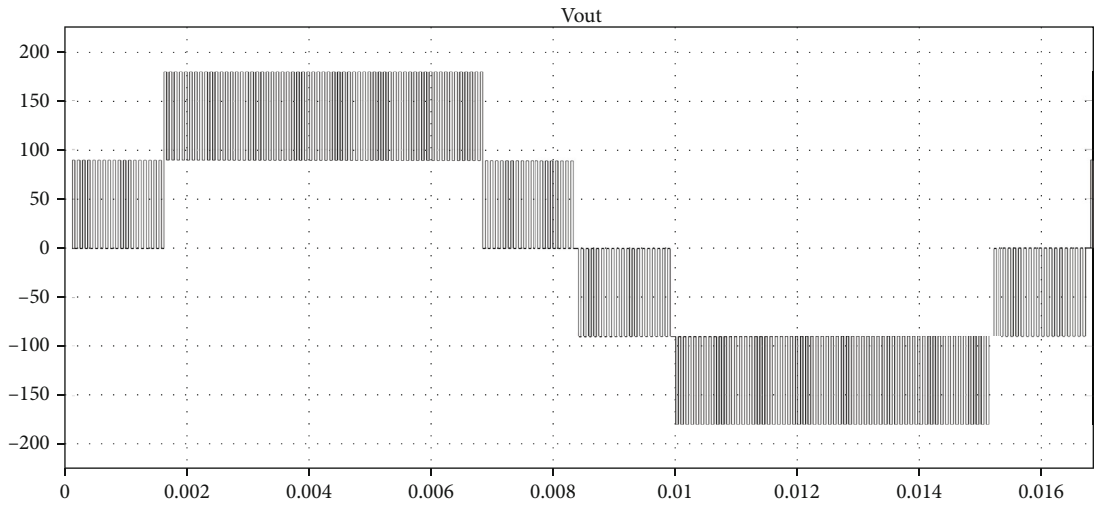


Figure 6: Output voltage waveform of proposed inverter without LC filter.

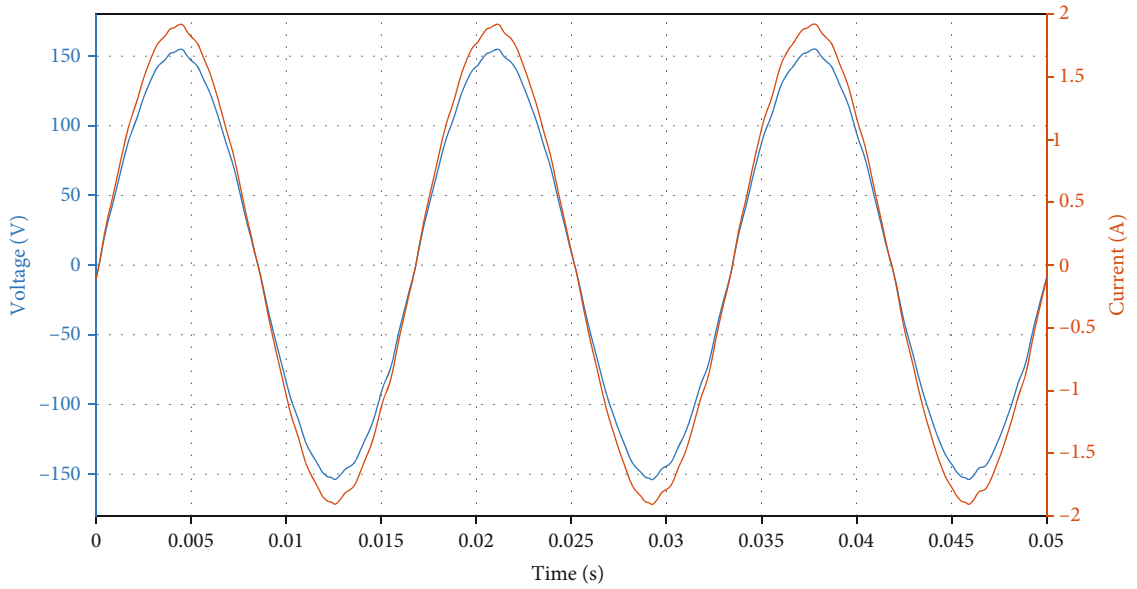


Figure 7: Output voltage and current waveform with LC filter.

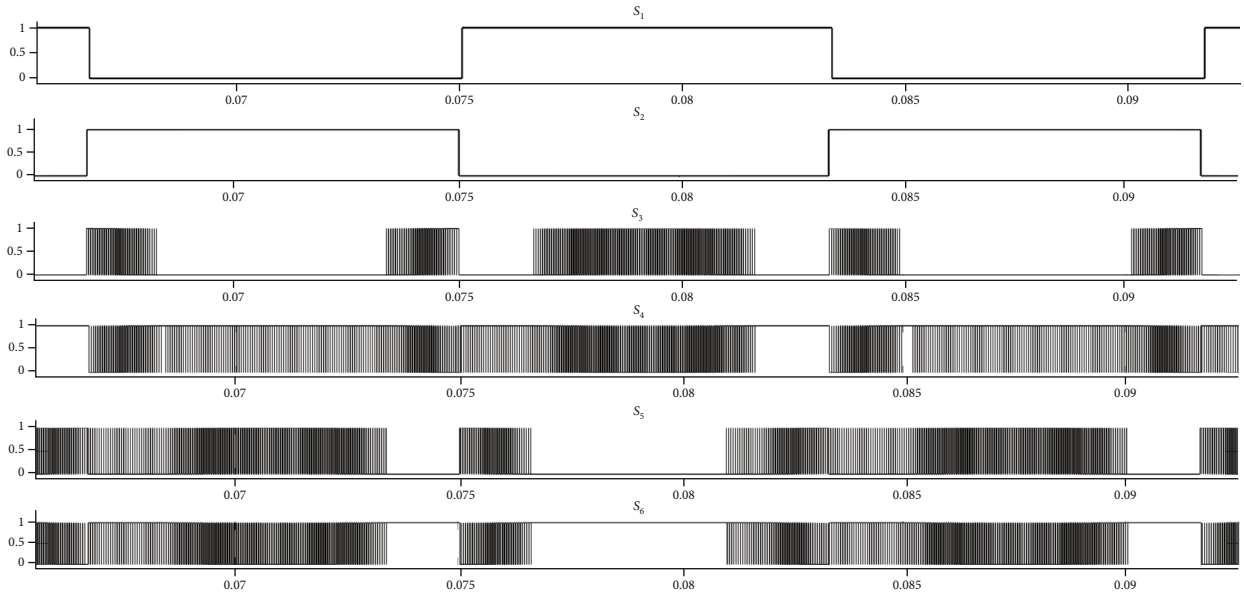


Figure 8: S_1-S_6 switching gate signals.

Table 3: Comparison between the proposed topology and some of the presented structures.

Five-level MLI	DC sources	Switch × breakdown voltage	Price
[12]	$2 \times (V_{DC}/2)$	$4 \times (V_{DC}/2)$, $4 \times V_{DC}$	$8 \times SW + 2 \times SD$
[13]	$1 \times (V_{DC})$	$4 \times (V_{DC}/2)$, $2 \times V_{DC}$	$6 \times SW + DI + 2 \times C + SD$
[14]	$4 \times (V_{DC}/2)$	$8 \times (V_{DC}/2)$	$8 \times SW + 4 \times SD$
[15]	$2 \times (V_{DC}/2)$	$1 \times (V_{DC}/2)$, $4 \times V_{DC}$	$5 \times SW + 4 \times DI + 2 \times SD$
[16]	$1 \times (V_{DC})$	$2 \times (V_{DC}/2)$, $4 \times (V_{DC})$	$6 \times SW + 2 \times DI + 2 \times C + SD$
[17]	$2 \times (V_{DC}/2)$	$2 \times (V_{DC}/2)$, $4 \times (V_{DC})$	$6 \times SW + 2 \times SD$
[18]	$1 \times (V_{DC})$	$2 \times (V_{DC}/2)$, $4 \times (V_{DC})$	$6 \times SW + 2 \times C + SD$
[19]	$1 \times (V_{DC})$	$8 \times (V_{DC}/2)$	$8 \times SW + 4 \times DI + 2 \times C + SD$
NPC	$4 \times (V_{DC}/2)$	$2 \times (2\,V_{DC})$, $2 \times (1.5\,V_{DC})$, $2 \times (V_{DC})$, $2 \times (V_{DC}/2)$	$8 \times SW + 6 \times DI + 4 \times SD$
FC	$2 \times (V_{DC})$	$2 \times (2\,V_{DC})$, $2 \times (1.5\,V_{DC})$, $2 \times (V_{DC})$, $2 \times (V_{DC}/2)$	$8 \times SW + 3 \times C + 2 \times SD$
CHB	$2 \times (V_{DC}/2)$	$8 \times (V_{DC}/2)$	$8 \times SW + 2 \times SD$
Proposed	$1 \times (V_{DC})$	$3 \times (V_{DC}/2)$, $3 \times V_{DC}$	$6 \times SW + 2 \times C + SD$

SW: price of an IGBT switch + gate driver; SD: price of DC sources; DI: price of a diode; C: price of a capacitor.

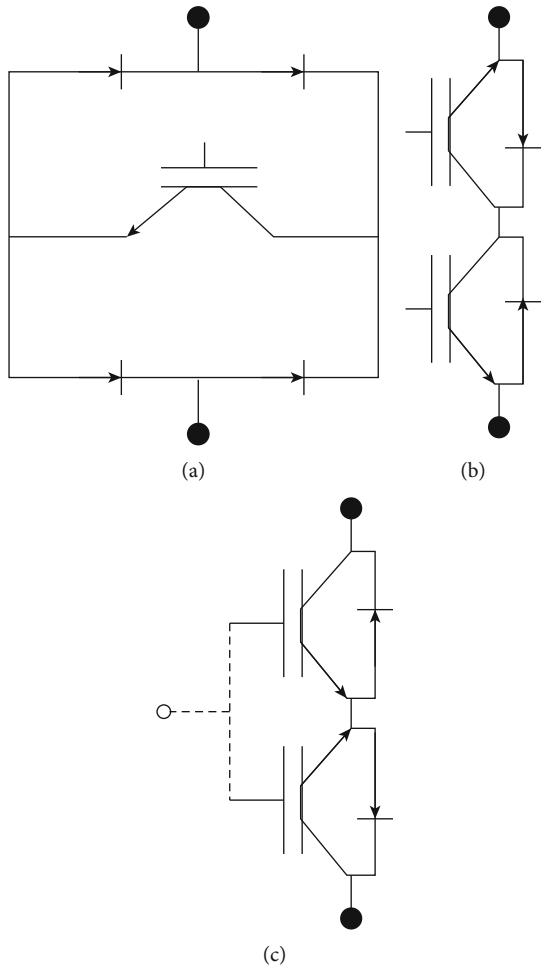


Figure 9: Bidirectional switches: (a) DE_IGBT: diode-embedded IGBT; (b) CC_IGBT: common collector; (c) CE_IGBT: common emitter.

Table 4: Comparison between Γu inverter and some of topologies.

Five-level MLI	Maximum conduction losses	Switch type	
[12]	4 × SW	4 × L	4 × H
[13]	4 × SW	4 × L	2 × H
[14]	2 × SW	—	8 × H
[15]	2 × SW + 2 × DI	2 × L	3 × H
[16]	3 × SW + DI	4 × L	2 × H
[17]	3 × SW	2 × L	4 × H
[18]	3 × SW	2 × L	4 × H
[19]	4 × SW	—	8 × H
NPC	4 × SW	—	8 × H
FC	4 × SW	—	8 × H
CHB	4 × SW	—	8 × H
Proposed	3 × SW	2 × L	4 × H

L: low-frequency switch; H: high-frequency switch.

Table 5: Comparison between losses.

Five-level MLI	Switching loss (w)	Conduction loss (w)	Total loss (w)
Unipolar	16.9	27.1	44
[15]	10.7	36	46.7
[16]	6.5	42	48.5
[17]	6.4	35.7	42.1
Proposed	9.1	32.4	41.5

Section A: in this section, amplitude of the inverter reference, V_r, is located between 0.5 V_{DC} and V_{DC} or V_5 and V_6, respectively. The switching time, T, is divided between these two effective vectors according to Equation (2).

$$V_r T = V_6 T_1 + V_5 T_2 = \frac{V_{DC}}{2} T_1 + V_{DC} T_2,$$

$$\begin{cases} T_1 = \left(2 - \dfrac{2V_r}{V_{DC}}\right) T, \\ T_2 = \left(\dfrac{2V_r}{V_{DC}} - 1\right) T. \end{cases} \tag{2}$$

Section B: when the inverter reference voltage, V_r, is between 0.5 V_{DC} and zero or V_4 and V_5, respectively, the switching times are divided between these two effective vectors according to Equation (3), where T_1 and T_2 are the duty cycles of the zero voltage vector and 0.5 V_{DC} level, respectively.

$$V_r T = V_4 T_1 + V_5 T_2 = \frac{V_{DC}}{2} T_2,$$

$$\begin{cases} T_1 = \left(1 - \dfrac{2V_r}{V_{DC}}\right) T, \\ T_2 = \left(\dfrac{2V_r}{V_{DC}}\right) T. \end{cases} \tag{3}$$

Section C: when the inverter reference vector, V_r is between -0.5 V_{DC} and zero voltage vector or V_4 and V_2, respectively. According to Equation (4), T_1 and T_2 are duty cycles of zero voltage vector and -0.5 V_{DC} level, respectively.

$$V_r T = V_4 T_1 + V_2 T_2 = -\frac{V_{DC}}{2} T_2,$$

$$\begin{cases} T_1 = \left(1 + \dfrac{2V_r}{V_{DC}}\right) T, \\ T_2 = \left(-\dfrac{2V_r}{V_{DC}}\right) T. \end{cases} \tag{4}$$

Section D: when the amplitude of the inverter reference voltage is between -0.5 V_{DC} and -V_{DC} voltages or V_1 and V_2, respectively, switching times are divided between these

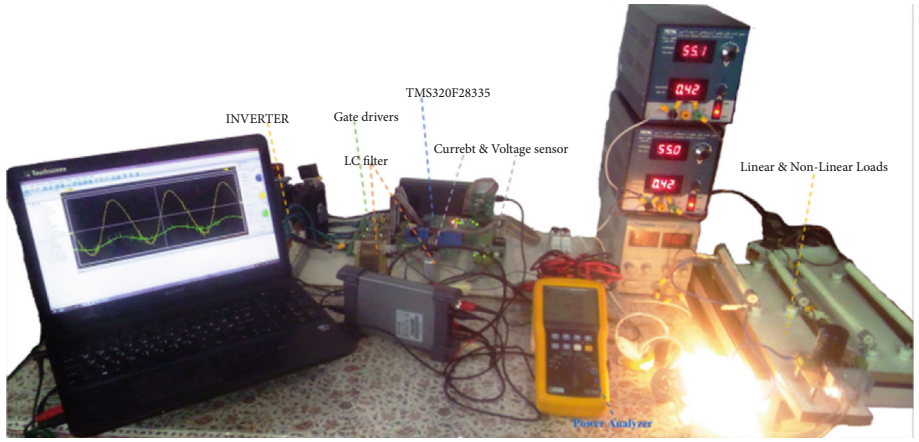


Figure 10: Γu converter prototype.

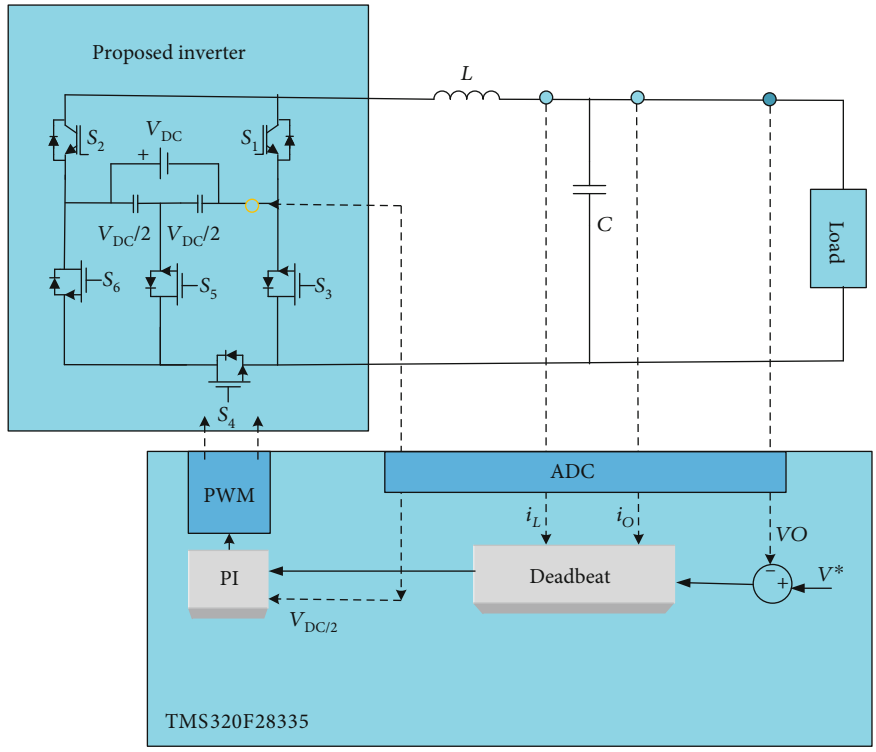


Figure 11: DC link capacitor voltage and deadbeat compensator.

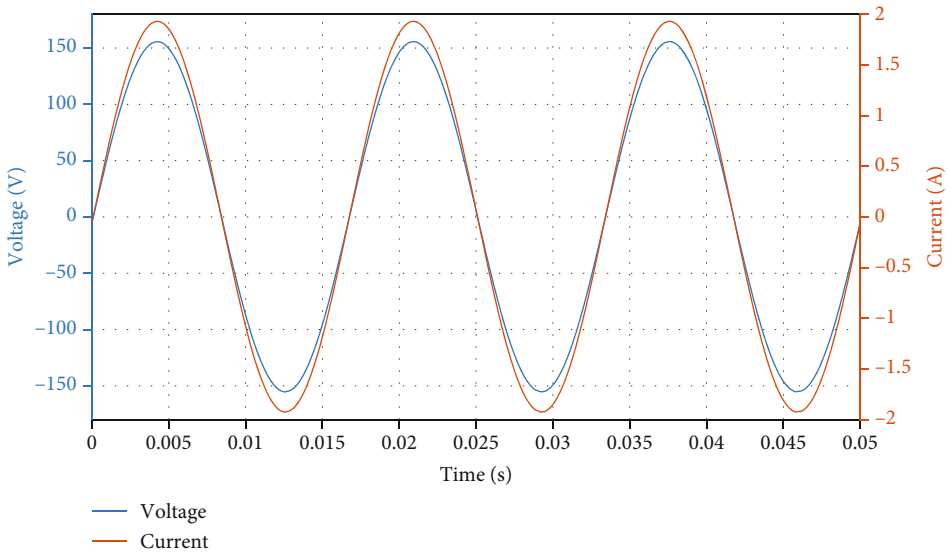


Figure 12: Linear load simulation result. $V_{DC} = 180$, VAC = 110, and THD $v = 0.5\%$.

two vectors according to Equation (5), where T_1 is the duty cycle of -0.5 V_{DC} and T_2 is the duty cycle of -V_{DC} level.

$$V_r T = V_2 T_1 + V_1 T_2 = -\frac{V_{DC}}{2} T_1 - V_{DC} T_2,$$

$$\begin{cases} T_1 = \left(2 + \dfrac{2V_r}{V_{DC}}\right) T, \\ T_2 = -\left(\dfrac{2V_r}{V_{DC}} + 1\right) T. \end{cases} \quad (5)$$

Due to the symmetry of the positive and also negative cycles of the sinusoidal waveform and inverter operation, at linear loads, the voltage of C_1 and C_2 capacitors will be almost balanced and there is no need for a voltage sensor or compensator design as shown in Figure 4. However, from experience, the voltage of capacitors can hardly be balanced in practical application due to the nonideal factors of inverter and nonlinear load. By changing the duty cycle of the activated voltage vectors, the voltage can be balanced. Therefore, a proportional integral (pi) compensator and control loop are proposed in Figure 5 for voltage balancing.

4. Open-Loop Simulations

Open-loop simulations for Γu inverter in MATLAB software are performed using the space vector pulse width modulation and based on the parameters in Table 2.

Figure 6 shows the five-level voltage waveform of the proposed converter.

Figure 7 shows the filtered voltage waveform and the output current of the converter. The simulations demonstrate that the voltage total harmonic distortion is 1.25%.

Figure 8 depicts the gate switching signals. In this figure, the switching frequency of S_1, S_2 switches is 60 Hz, and in the S_5, S_6, average switching frequency is 14670 Hz and average switching frequency of S_3, S_4 is

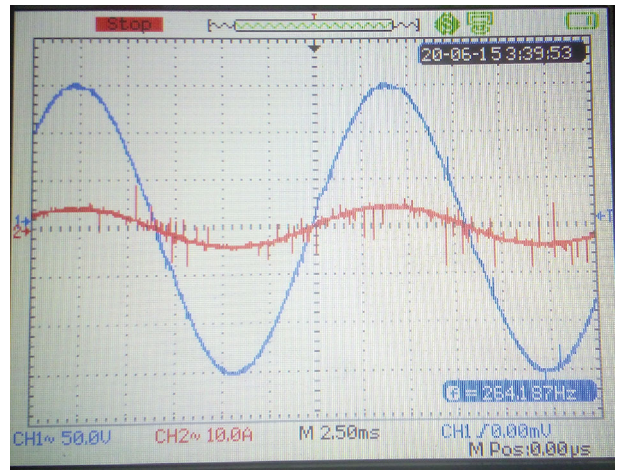


Figure 13: Linear load experimental result.

16680 Hz. The S_1, S_2 switches are switching in fundamental frequency. Reducing the switching frequency is improving the converter efficiency, so low-switching semiconductors such as IGBTs or GTOs are applicable for this segment, but in the S_3-S_6, high-frequency switches like MOSFETs can be used.

As shown in Figure 4, the voltage ripple of the capacitors is reasonable, and this voltage is stabilized without any compensation in open-loop simulation.

Criteria such as the number of switches, independent DC voltage sources, capacitor clamps, and diode clamps about device counts are definable [11]. Furthermore, breakdown voltages of the switches, switching frequency, and converter controllability are determinable. According to Table 3, the Γu5L inverter has the advantage of implements with a single DC source and without transformer and clamping diodes. Therefore, this topology is a suitable MLI with the advantage of reducing device counts.

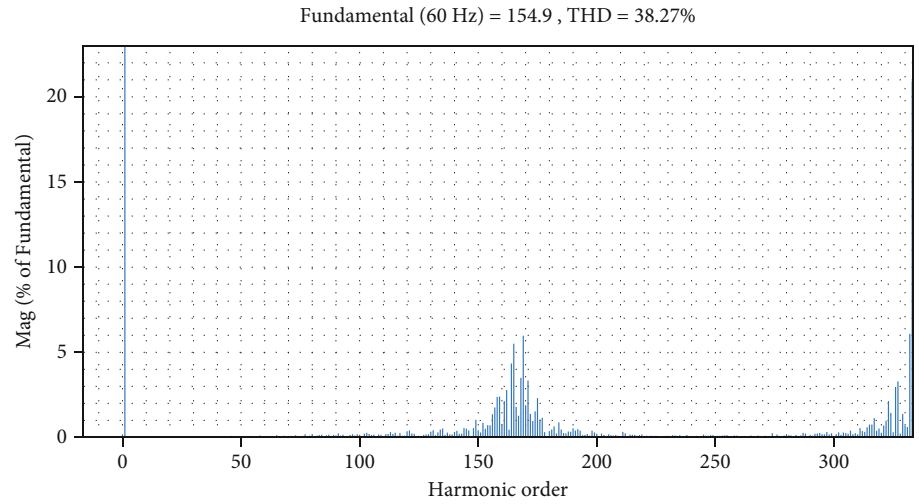


Figure 14: The closed-loop voltage FFT before filter.

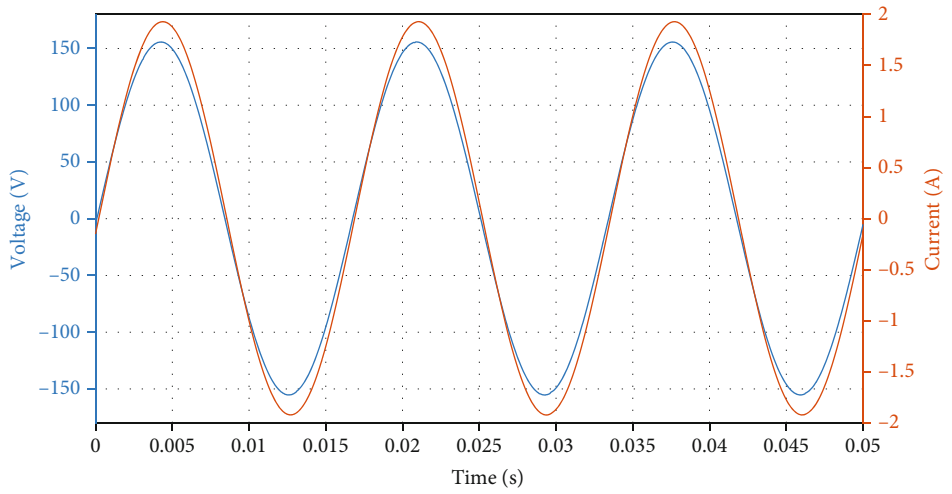


Figure 15: RL load simulation result. $V_{DC} = 180$, VAC = 110.1, THD $v = 0.6\%$, $R = 80\,\Omega$, and $L = 10$ mH.

NPC, FC, and CHB require several isolated DC voltage sources and transformers, which have increased their cost and mass compared to Γu inverter [12, 14, 17].

Inverter [18] has four high breakdown voltage switches, but the Γu5L inverter has three switches, which means more switch prices and according to the equal number of commutations means higher switching losses.

The bidirectional switches have different varieties; some of which are shown in Figure 9. In comparison, DE_IGBT has the highest conduction losses between all types of bidirectional switches. Although the topology [15] has a five IGBT but due to the presence of DE_IGBT, this structure has four more diodes and more losses. The CC_IGBT is implemented with two unidirectional switches, and it requires two gate drivers.

Fault detection in MLI is an important and complex issue. Industrial gate drivers require a collector-emitter voltage sample. When the IGBT is in an overcurrent condition, the DESAT (VCE) exceeds an internal reference voltage; in this time, gate driver applies soft turn off, so isolated pulse generators as gate drivers do not have DESAT protection; because of this, in T5MLC [14] and T-type [18]topologies, two gate drivers with error detection capability are considered for each CC_IGBT or CE_IGBT bidirectional switch.

Classic five-level inverters NPC, FC, and CHB have eight high-frequency switches with maximum of four switch conductions in each level that increase the cost and conduction losses. According to Table 4, the proposed topology has four high-frequency switches. In comparison with conventional five-level structures, the proposed topology has two low-frequency switches, which reduce the switching loss of MLI . At each level, maximum of three conducts and three changes occurred. Regarding a smaller number of conduction and commutation, conduction and switching losses decreased.

Because of fundamental switching frequency for high blocking voltage switches leg and reducing switching losses due to the three-level structure on the other leg, the efficiency of this converter is higher than the conventional two-level inverters. According to the test conditions in [17], simulations of losses have been performed and comparison of losses is shown in Table 5.

5. Proposed Control Method for Γu Inverter

In inverters, due to the nonlinear current passing through the LC filter and applying dead time during switching, the waveform becomes nonsinusoidal. The task of removing the high-frequency harmonics is the responsibility of the LC filter and controlling the low-voltage harmonics of the compensator. The filter inductor is calculated as follows:

$$L = \frac{V_{\mathrm{DC}}}{4f_S \times \Delta I_{lp-p}}, \tag{6}$$

whereΔI_{lp-p} is the peak-to-peak inductor current and f_S is the switching frequency. The capacitor is also designed to have a cut-off frequency at least ten times smaller than the inverter switching frequency. The filter capacitor is calculated as follows:

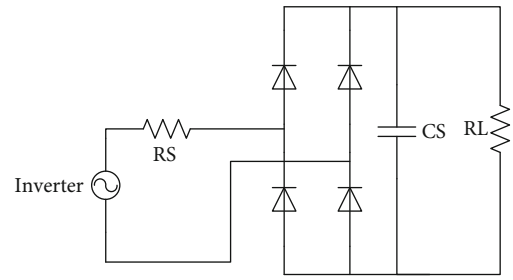


Figure 16: Nonlinear load test. RL = 272 Ω, CS = 458 μF, and RS = 4.8 Ω.

$$f_C = \frac{1}{2\pi\sqrt{\mathrm{LC}}}. \tag{7}$$

Deadbeat (DB) has a rapid dynamic, low-computation digital control method based on a discrete-time model of the system. The deadbeat is a stabilize closed-loop system. The positioning of the poles is located at the center of the z plane and within the unit circle [20]. The inverter state-space model is determined based on LC filter parameters and inductor current and capacitor voltage. The load current is considered as a disturbance. The values of matrices A, B, and D are as follows:

$$\frac{d}{dt}\begin{bmatrix} I_L \\ V_o \end{bmatrix} = A\begin{bmatrix} I_L \\ V_o \end{bmatrix} + BV_i + DI_o,$$

$$A = \begin{bmatrix} 0 & \dfrac{-1}{L} \\ \dfrac{1}{C} & 0 \end{bmatrix},$$

$$B = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix},$$

$$D = \begin{bmatrix} 0 \\ \dfrac{-1}{C} \end{bmatrix}. \tag{8}$$

The KVL and KCL equations for the converter are as follows:

$$\begin{cases} \mathrm{KCL} \Rightarrow I_c = C\dfrac{dv_o}{dt} = I_L - I_o, \\ \mathrm{KVL} \Rightarrow V_i = L\dfrac{dI_L}{dt} + V_o \Rightarrow L\dfrac{dI_L}{dt} = V_i - V_o. \end{cases} \tag{9}$$

According to the sampling time (Ts) in Equation (9), discrete time derivative is as follows.

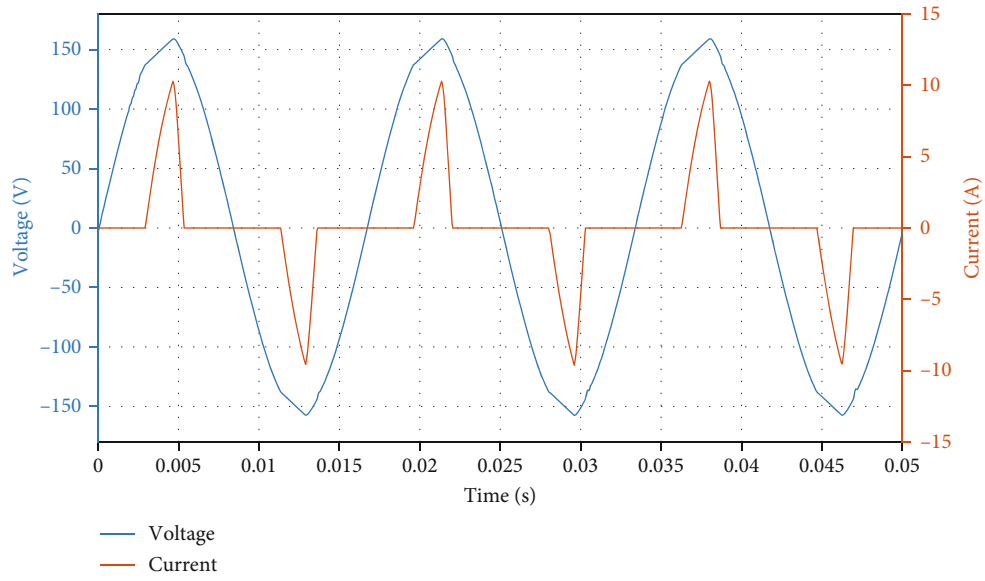


Figure 17: Nonlinear load simulation results. $V_{DC} = 180$, VAC = 110, and THD $v = 2.6\%$.

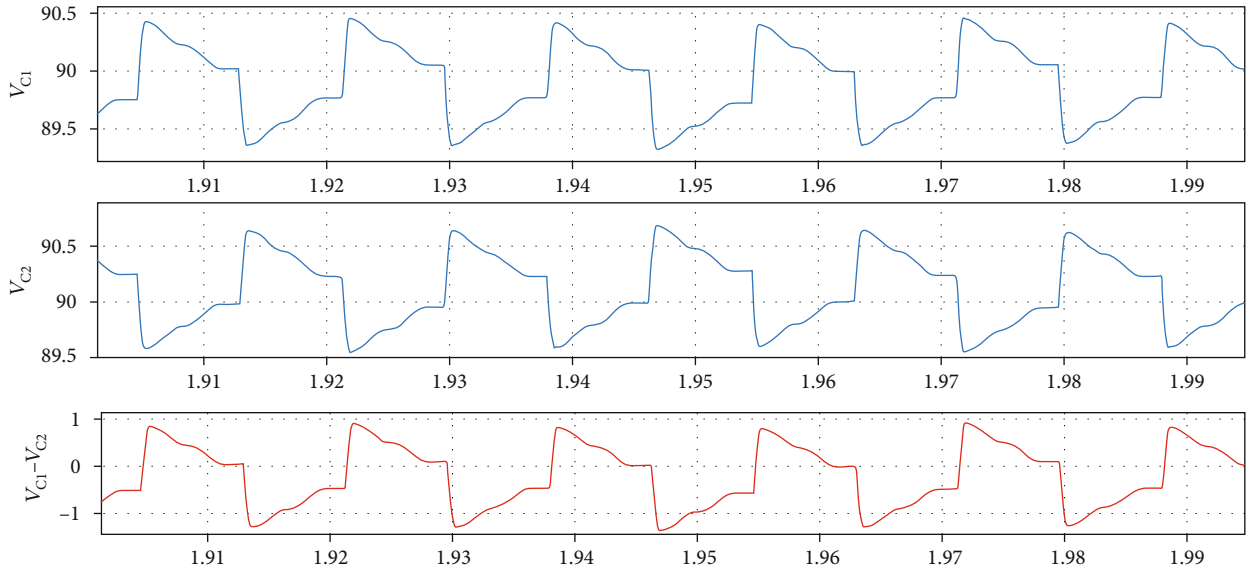


Figure 18: DC link capacitor voltage in nonlinear load.

$$\begin{cases} \dfrac{I_L(z+1)-I_L(z)}{Ts} = \dfrac{1}{L}[V_i(z)-V_o(z)], \\ \dfrac{V_o(z+1)-V_o(z)}{Ts} = \dfrac{1}{C}[I_L(z)-I_o(z)]. \end{cases} \tag{10}$$

The state variables at time $z+1$ are as follows:

$$\begin{cases} I_L(z+1) = I_L(z) + \dfrac{1}{Lf_s}[V_i(z)-V_o(z)], \\ V_o(z+1) = V_o(z) + \dfrac{1}{Cf_s}[I_L(z)-I_o(z)] = V_o(z) + \dfrac{1}{Cf_s}I_c(z). \end{cases} \tag{11}$$

The state variables in the next sampling time $z+2$ are as follows:

$$\begin{cases} I_L(z+2) - I_L(z+1) = \dfrac{1}{Lf_s}[V_i(z+1)-V_o(z+1)], \\ [V_o(z+2) - V_o(z+1)] = \dfrac{1}{Cf_s}I_c(z+1). \end{cases} \tag{12}$$

If the high sampling frequency is selected, the voltage and current changes can be considered linear and can be written as follows:

$$\begin{cases} [I_L(z+1) - I_L(z)] = \dfrac{1}{Lf_s}[V_i(z+1)-V_o(z+1)], \\ [V_o(z+1) - V_o(z)] = \dfrac{1}{Cf_s}I_c(z+1). \end{cases} \tag{13}$$

In the DB method, the values of $z+1$ are the same as the reference values, so the reference values of the output voltage and the reference capacitors and inductor currents at time Z can be written as follows:

$$\begin{cases} V_i^*(z) = V_o^*(z) + Lf_s[I_L^*(z) - I_L(z)], \\ I_L^*(z) = I_o(z) + Cf_s[V_o^*(z) - V_o(z)]. \end{cases} \tag{14}$$

Compared to the model predictive control MPC method, DB has two advantages of reducing compute volume and constant switching frequency. The MPC method requires the calculation of the cost function and the selection of the optimal vectors, so in this method, the switching frequency is variable. However, in the DB method, the computation volume is low, and the inverter reference voltage is generated by the modulator. Hence, the switching frequency is constant, and the modulator also makes the LC filter easier to design.

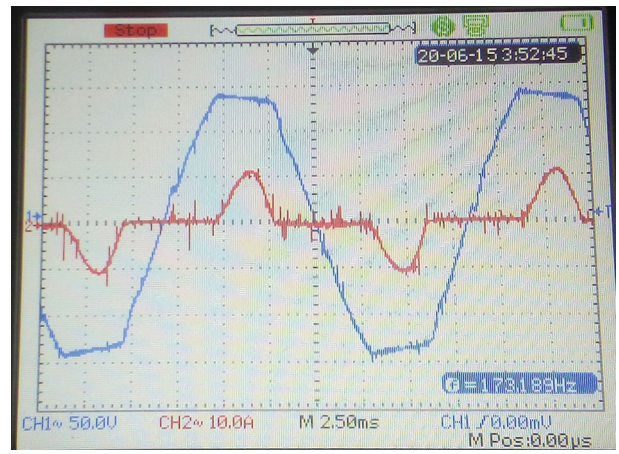


Figure 19: Nonlinear load experimental results.

6. Closed-Loop Simulation and Experimental Results

The compensator must stabilize the amplitude of the main component of the voltage in all conditions and provide the required current for linear and nonlinear loads.

The closed-loop Γu5L inverter is implemented based on the parameters in Table 2.

The prototype is illustrated in Figure 10, which achieved a closed-loop system according to Figure 11, using a TMS320F28335 floating-point TI DSP and LUH100G1202 IGBT modules. The Hantek 6022BE PC-Based USB Digital Oscilloscope and Chauvin Arnoux C.A 8220 power analyser are used to sample the prototype's voltage, current, and total harmonic distortion waveforms.

The response of the inverter Γu5L is investigated by applying the linear and nonlinear loads.

6.1. Linear Load Closed-Loop Simulation and Experimental Results. The simulation and the experimental results of the linear resistive load for the Γu5L inverter are illustrated in Figure 12 and Figure 13, and laboratory prototype results confirm the simulation results.

The closed-loop voltage FFT of the Γu inverter before the LC filter is illustrated in Figure 14, which shows the proper design of the DB controller and the LC filter. The LC filter is responsible for removing high-frequency harmonics, and the compensator is responsible for controlling low-frequency harmonics. The filter reduces the voltage total harmonic distortion from 38.27% to 0.5% to comply with IEC 62040-3.

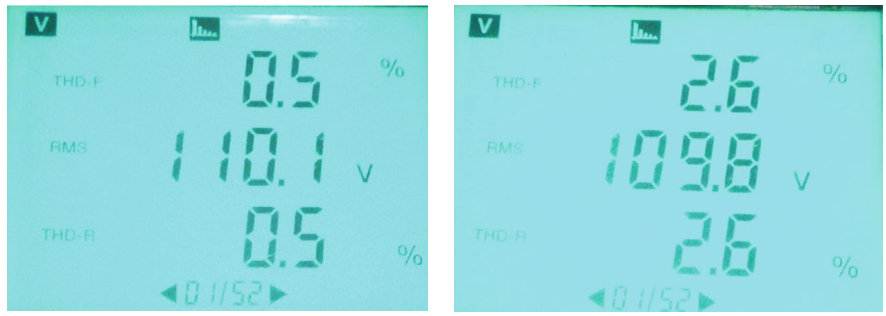
In order to investigate the linear inductive loads, the RL load simulation is performed as follows: the voltage and current waveform is as Figure 15.

6.2. Nonlinear Load Closed-Loop Simulation and Experimental Results. According to IEC620-40-3, the nonlinear load parameters can be defined as follows in Figure 16:

The simulation and the experimental results for the nonlinear load are represented in Figures 17–19, and laboratory prototype results confirm the simulation results.

Table 6: Standard limit and individual harmonic of Γu inverter.

Even harmonic			Odd harmonic		
Harmonic order	IEC62040-3%	Γu inverter %	Harmonic order	IEC62040-3%	Γu inverter %
2	2	0.11	3	5	0.66
4	1	0.24	5	6	1
6	0.5	0.14	7	5	1.02
8	0.5	0.12	9	1.5	0.71
10	0.2	0.09	11	3.5	0.38
12	0.2	0.05	13	3	0.12
14	0.2	0.09	15	0.3	0.14
16	0.2	0.04	17	2	0.11
18	0.2	0.06	19	1.5	0.09
20	0.2	0.03	21	0.2	0.05
22	0.2	0.03	23	1.5	0.06
24	0.2	0.03	25	1.5	0.03



(a) (b)

Figure 20: Experimental THD in linear load (a) and nonlinear load (b).

The THD value calculated before the LC filter is 45% for nonlinear load and 38.2% for linear load using MATLAB FFT analysis. The comparison between standard limit and individual harmonic value of the Γu5L inverter at the nonlinear load in laboratory prototype test is shown in Table 6. According to Figure 20, voltage total harmonic distortion less than 0.6% at linear load and voltage total harmonic distortion less than 2.6% at nonlinear load indicate compliance with IEC620-40-3 [21].

7. Conclusion

In this paper, the following works have been done and new results have been obtained, which are as follows:

(1) Γu inverter is proposed that has less devices with a single DC voltage source and does not require clamping diodes. This transformerless structure reduces the installation space and weight. Also, this converter has self-balanced capacitor voltage property under linear loads. Results show that the efficiency of this converter is higher than the conventional five-level and two-level inverters

(2) Single-phase five-level space vector pulse width modulation for Γu5L inverter was proposed. This technique reduces the complexity of modulation implementation

(3) According to the proposed balancing method, there is no need for two independent sources, and the structure can be controlled with two bulk capacitors

(4) Two predictive control methods are analysed for Γu5L inverter, and a rapid dynamic, low-computation cost digital control method with SVPWM modulator, and constant switching frequency was proposed for closed-loop control

(5) The performance of the proposed converter under nonlinear and linear loads was confirmed by performing an analytical study, including simulation and an experimental result

(6) According to test results, it was shown that voltage total harmonic distortion becomes less than 1% at linear load and voltage total harmonic distortion is less than 3% at nonlinear load, which indicates compliance with the sensitive critical loads standard in standalone photovoltaic inverters

Data Availability

All the data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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