Design of Reversible Decoder in the Quantum Cellular Automata (QCA) Technology

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Abstract

MOSFET technology comes with a number of disadvantages, including tunneling and overheating. So researchers are looking for alternatives to MOSFET technology. One of these technologies is Quantum Cellular Automata Circuits (QCA), which offers a new method for calculating nanotechnology. Also, given the growing importance of reducing energy consumption, the use of reversible logic in QCA technology is a new issue. One way to solve the power loss problem is to design the circuits in a reversible manner. Circuit design using reversible gates ensures that the circuit does not waste energy. And by using fault tolerance mechanisms, it prevents bit errors. In this paper, the reversible decoder was designed and simulated using QCA Designer software. Due to the main property of reversible circuits, power consumption is also reduced. And by using fault tolerance mechanisms, it prevents bit errors.

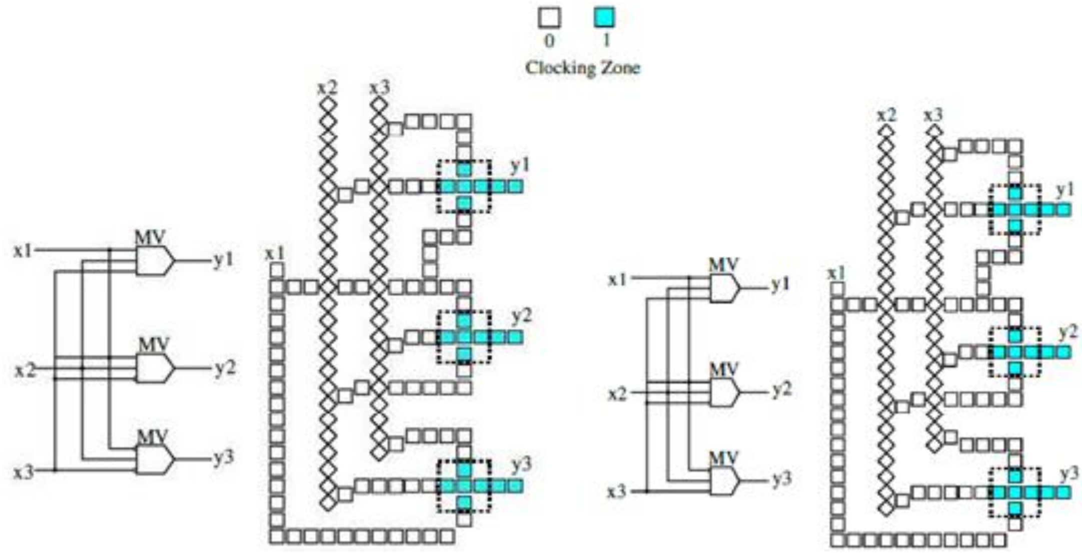
Key words: Reversible, Decoder, Quantum cellular automata, Power consumption, Error

1. Introduction

According to the unique features that is in reducing size in nanotechnology, this technology provides new opportunities for calculating. Heretofore, new parts are designed such as carbon nanotubes, single electron transistors, resonance tunneling diodes, Single molecular components and spin transistors. It is expected that using these new components simultaneously can achieve super-high density and ultra-high speed. Today, the possibility of reducing transistors and installing more of them on the chip in CMOS technology has been confronted with Limitations, and the feasibility of Moore's law in the near future comes with suspicion. Therefore, researchers are looking for technologies with smaller size, less consumption power [1]. Quantum dote-Cellular Automata (QCA) is not only a Nano-scale solution, but also provides a new method for calculating and transfer information. Consider the characteristics of the processing of CMOS systems: Some circuits, for example, logic gates, perform calculations; while others, such as wires for signal / data transmission, as well as for communications, are used. Conversely, computing and communication are done simultaneously in the QCA. In QCA, it is used two base logic gates the INV inverse and the MAJ majority gate. QCA technology is very promising, because with this technology, computing patterns that are essentially extracted from traditional CMOS can be implemented. The QCA design includes a variety of new and emerging examples such as dynamic memory and processing with wire. One thing to keep in mind is that each gate and structure that can perform a specific action on inputs and deliver on outputs or outputs is not unique, and there are several different structures that can do the same. This helps to examine the advantages and disadvantages of each structure, and each one in the right place and in order to take advantage of that structure.

2.Reversible circuits based on QCA

One of reversible gate ways is to use QCA structures. Reversible calculations are considered as the proper solution to prevent lost energy and states that since computations are performed at the logical level and at the same time it is possible to detect errors in Circuit output is there, therefore, we do not Loss of information [3]. Two QCA1 and QCA2 structures, as shown in Figure 1, are two reversible gates with a QCA structure, and are the basis for work in the field of making reversible circuitry with QCA technology.



a. QCA1 gate design [3] **b.** QCA2 gate design [3] **Figure 1.**

The QCA1 and QCA2 gate input and output relationships are respectively in accordance with formulas 1 and 2.

$$y1 = M(x1, x2, x3) = x1x2 + x2x3 + x1x3$$

$$y2 = M\ (x1, x2, \overline{x3}) = x1x2 + x2\overline{x3} + x1\overline{x3} \qquad (1)$$

$$y3 = M\ (\overline{x1}, x2, x3) = \overline{x1}x2 + x2x3 + \overline{x1}x3$$

$$y1 = M\ (x1, x2, x3) = x1x2 + x2x3 + x1x3$$

$$y2 = M\ (x1, x2\ ,\overline{x3}) = x1x2 + x2\overline{x3} + x1\overline{x3} \qquad (2)$$

$$y3 = M\ (\overline{x1}, x2,\overline{x3}) = \overline{x1}x2 + x2\overline{x3} + \overline{x1}\overline{x3}$$

In Table 1, four gates of Fredkin and Toffoli, QCA1 and QCA2 have been compared. We see that these two structures are superior to common gateways in reversible circuits for implementation with QCA cells.

Table 1. Comparison between four reversible gates [3]

	Fredkin	Toffoli	QCA1	QCA2
Clock Zones	4	4	2	2
MVs	6	4	3	3
Area	30 * 18	31*18	27*15	27*15
Control cells	6	2	0	0
Normal Cells Non-rotated rotated	185 122 63	167 140 27	146 100 46	146 100 47

In table 2, we encountered an error of Lack of cell placement for two Fredkin, Tufoli gates, if implemented with QCA technology. First, for the plan of the Fredkin gate structure with QCA cells, fourteen patterns of error of Lack of cell placement are considered. In the upper row of the table, the Lack of cell placement of each of these patterns in the structure is specified by a number from 1 to 14.

So, the eight input modes 000 to 111 can be applied that they are shown with 0a Up to 7a. In the two columns on the left side of the table, we have the Intended input and output vector without error. now, we can see the gate output in the event of an error of Lack of cell placement of Each one of the fourteen error patterns in it in case of you do in each of the eight input modes and you can compare it with the output value without Intended error. The same is seen in Table 2 for the Tufoli gate, which has thirteen error patterns for the QCA structure.

Table2. Error of Lack of cell placement in two Gates of Fredkin and Tufoli [3]

Fredkin Gate															
Input Vector	Fault Free	FP													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
a_0	a_0	a_0	a_1	a_1	a_0	a_1	a_0	a_1	a_2	a_2	a_0	a_0	a_2	a_2	a_0
a_1	a_2	a_3	a_3	a_3	a_2	a_3	a_3	a_3	a_2	a_2	a_3	a_2	a_2	a_0	a_2
a_2	a_1	a_1	a_1	a_1	a_1	a_1	a_1	a_0	a_3	a_3	a_1	a_1	a_3	a_3	a_3
a_3	a_3	a_3	a_3	a_3	a_3	a_3	a_3	a_2	a_3	a_3	a_3	a_3	a_3	a_1	a_3
a_4	a_4	a_4	a_5	a_4	a_4	a_5	a_4	a_4	a_4	a_6	a_4	a_4	a_6	a_4	a_4
a_5	a_5	a_5	a_5	a_5	a_4	a_4	a_4	a_5	a_5	a_7	a_5	a_5	a_7	a_5	a_5
a_6	a_6	a_6	a_7	a_6	a_6	a_7	a_6	a_6	a_6	a_6	a_6	a_4	a_4	a_6	a_4
a_7	a_7	a_7	a_7	a_7	a_6	a_6	a_6	a_7	a_7	a_7	a_7	a_5	a_5	a_7	a_5
Toffoli Gate															
Input Vector	Fault Free	FP													
		1	2	3	4	5	6	7	8	9	10	11	12	13	
a_0	a_0	a_0	a_4	a_0	a_4	a_0	a_0	a_0	a_4	a_0	a_4	a_0	a_4	a_0	
a_1	a_1	a_1	a_5	a_1	a_1	a_1	a_1	a_1	a_5	a_1	a_5	a_5	a_1	a_1	
a_2	a_2	a_2	a_6	a_2	a_2	a_2	a_2	a_2	a_6	a_2	a_6	a_2	a_6	a_2	
a_3	a_7	a_7	a_7	a_3	a_3	a_7	a_7	a_3	a_7	a_3	a_7	a_3	a_3	a_7	
a_4	a_4	a_4	a_4	a_4	a_4	a_0	a_0	a_0	a_0	a_0	a_0	a_4	a_4	a_0	
a_5	a_5	a_5	a_5	a_5	a_5	a_5	a_1	a_1	a_5	a_1	a_1	a_5	a_1	a_5	
a_6	a_6	a_6	a_6	a_6	a_6	a_6	a_6	a_6	a_2	a_6	a_6	a_2	a_6	a_2	
a_7	a_3	a_7	a_7	a_3	a_3	a_7	a_3	a_3	a_7	a_7	a_7	a_3	a_3	a_7	

In Table 3, seven patterns of lines are considered for both 1QCA and 2QCA gates, and we see the results. in terms of resistance, A comparison can be made between these four gates against this error.

Table 3. Error of Lack of cell placement in two QCA1 and QCA2 gates [3]

QCA1 Gate								
Input Vector	Fault Free	FP_1	FP_2	FP_3	FP_4	FP_5	FP_6	FP_7
a_0	a_0	a_0	a_0	a_0	a_0	a_0	a_0	a_4
a_1	a_1	a_0	a_0	a_1	a_1	a_3	a_1	a_1
a_2	a_3	a_3	a_3	a_3	a_1	a_3	a_7	a_7
a_3	a_5	a_5	a_4	a_7	a_5	a_7	a_5	a_5
a_4	a_2	a_2	a_3	a_0	a_2	a_0	a_2	a_3
a_5	a_4	a_4	a_4	a_4	a_6	a_4	a_0	a_0
a_6	a_6	a_7	a_7	a_6	a_6	a_4	a_6	a_6
a_7	a_7	a_7	a_7	a_7	a_7	a_7	a_7	a_3
QCA2 Gate								
Input Vector	Fault Free	FP_1	FP_2	FP_3	FP_4	FP_5	FP_6	FP_7

a_0	a_1	a_0	a_0	a_1	a_1	a_1	a_1	a_5
a_1	a_0	a_0	a_0	a_0	a_0	a_2	a_0	a_0
a_2	a_3	a_3	a_2	a_3	a_1	a_3	a_7	a_7
a_3	a_5	a_5	a_5	a_7	a_5	a_7	a_5	a_5
a_4	a_2	a_2	a_2	a_0	a_2	a_0	a_2	a_2
a_5	a_4	a_4	a_5	a_4	a_6	a_4	a_0	a_0
a_6	a_7	a_7	a_7	a_7	a_7	a_5	a_7	a_7
a_7	a_6	a_7	a_7	a_6	a_6	a_6	a_6	a_2

As shown in figure 2, we have reversible gate, that the input of Xn is entered in to it, and we received Yn outputs. If these outputs enter at the reversible gate R means R`, then the result will be that the first inputs of Xn. Then, in figure 3, we have Finman's reversible gate, which, as shown in figure 3b, if one of its inputs is set to zero, it acts like a buffer [4].

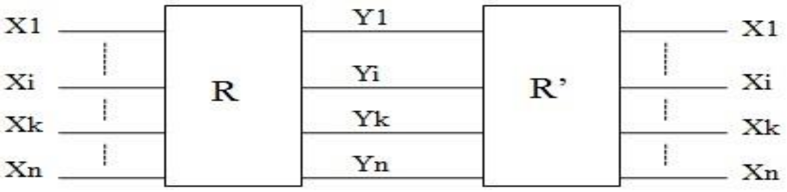
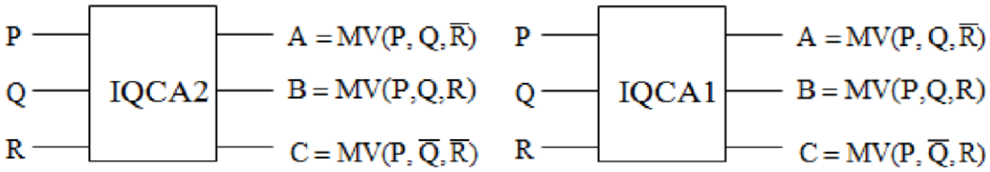


Figure 2. Connecting the two reversible Gates of the R sample and R` is the reverse it [4]

The main challenge in this article is that if we want to Get multiple outputs from the reversible gate, then the operation of the circuit will have an error. The solution is using each gate alongside its reverse and then getting help from the designed buffer to get multiple outputs. In this way, in the reversible gate output, we have that first input and can be applied to the circuit and at the same time we can have an instance of it to detect the error. You can use this method for each line.

As shown in Figure 3, we can design IQCA2 and IQCA1 gates for QCA1 and QCA2 gates as their reverse, and all circuits designed with them by helping the Presented buffer we can detection an error.



[4] **b.** Reversible Gate QCA [4] **Figure 3. a.** QCA 1 Reversible Gate

3. Reversible decoder

Due to the QCA1 reversible gate [3] and reversible circuits [4] and the input and output relationships of this gate, which are shown in Figures 1 and 2, a reversible decoder can be designed according to Figure 4. If a logical value of zero is applied to input A, it can be considered as a one-to-two decoder, where the input B will be the base of the activator and the input C will be the input of the decoder. And the correct table of proposed reversible decoder, is shown in Table 4.

With the help of two one-by-two decoders, a two-by-four decoder can be designed (Figure5). The design of this decoder simulated using the QCA Designer software, is shown in Figure 6.

Table 4. The correct table of proposed reversible decoder

A	B(En)	C(N_0)	Y_1	Y_0
0	0	0	0	0

0	0	1	0	0
0	1	0	0	1
0	1	1	1	0

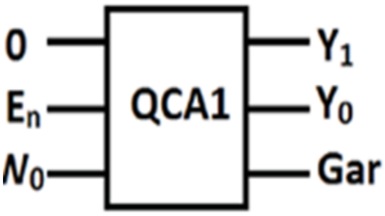
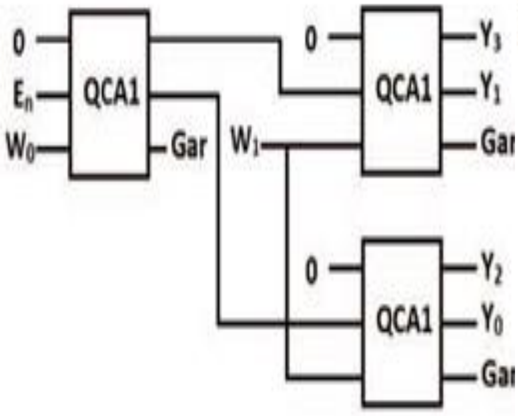


Figure 4. One to two decoder with 1QCA gate



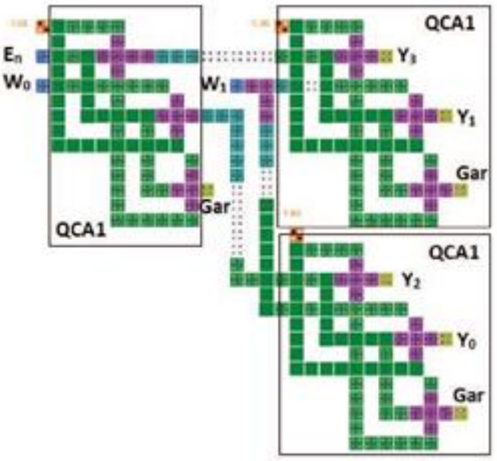


Figure 5. two-by-four decoder

Figure 6. QCA layout of full proposed reversible decoder circuit

4. Conclusion

One way to solve power loss and error reduction is to design the circuits in a reversible manner. Circuit design using reversible gates means that the circuit does not waste energy. They are,nt wasting energy, and this is a waste of energy due to the overlapping mapping between input and output vectors. Reversibility recovers lost energy and prevents bit errors by using fault tolerance mechanisms. In this paper, the reversible decoder was designed and simulated using QCADesigner software. And due to the main property of reversible circuits, power consumption and error are reduced.

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