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Design of reversible multiplexer 4*1 by multiplexer 2*1 in the quantum cellular automata (QCA) circuits

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Abstract

Quantum cellular automata (QCA) circuits are an alternative CMOS technology. Also, given the growing importance of reducing energy consumption, the plan of use reversible logic in QCA technology is a new issue, which reduces power dissipation in circuits.
*In this paper, a reversible multiplexer 4*1 circuit was designed, and this multiplexer is simulated using the QCA Designer software. Therefore, according to its reversibility, power consumption was reduced, and by error tolerance mechanisms, a bit error is prevented.*

Key words: *Reversible, Quantum cellular automata, Power consumption, Error, multiplexer*

1. Introduction

Today, the possibility of reducing transistors and installing more of them on the chip in CMOS technology has been confronted with Limitations, and the feasibility of Moore's law in the near future comes with suspicion. Therefore, researchers are looking for technologies with smaller size, less consumption power [1]. Quantum dote - Cellular Automata (QCA) is not only a Nano-scale solution, but also provides a new method for calculating and transfer information. Consider the characteristics of the processing of CMOS systems: Some circuits, for example, logic gates, perform calculations; while others, such as wires for signal / data transmission, as well as for communications, are used. Conversely, computing and communication are done simultaneously in the QCA. In QCA, it is used two base logic gates the INV inverse and the MAJ majority gate. QCA technology is very promising, because with this technology, computing patterns that are essentially extracted from traditional CMOS can be implemented. The QCA design includes a variety of new and emerging examples such as dynamic memory and processing with wire. One thing to keep in mind is that each gate and structure that can perform a specific action on inputs and deliver on outputs or outputs is not unique, and there are several different structures that can do the same. This helps to examine the advantages and disadvantages of each structure, and each one in the right place and in order to take advantage of that structure.

2.Reversible circuits based on QCA

One of reversible gate ways is to use QCA structures. Reversible calculations are considered as the proper solution to prevent lost energy and states that since computations are performed at the logical level and at the same time it is possible to detect errors in Circuit output is there, therefore, we do not Loss of information [2]. Two QCA1 and QCA2 structures, as shown in Figure 1, are two reversible gates with a QCA structure, and are the basis for work in the field of making reversible circuitry with QCA technology.

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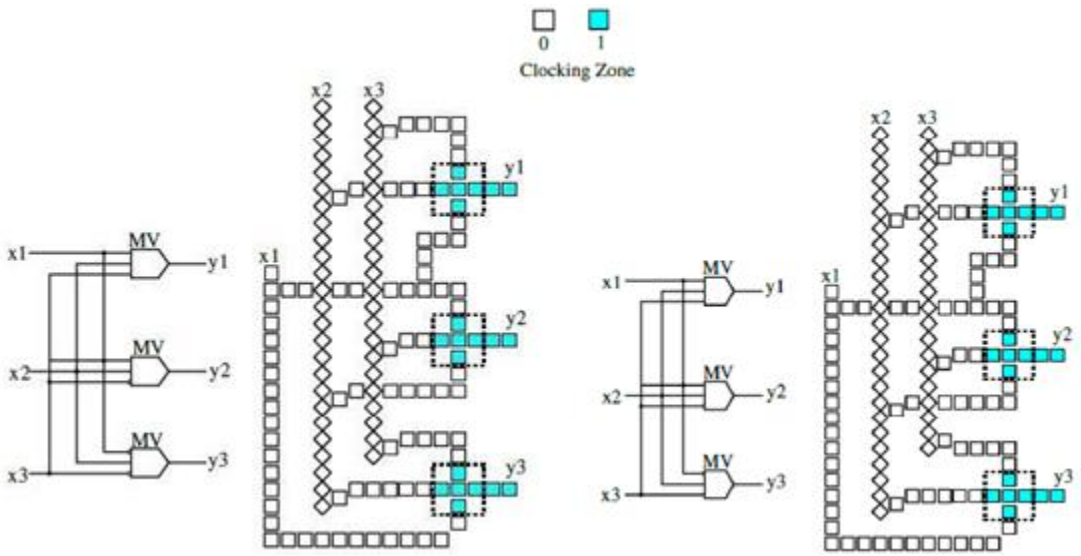

Figure 1. a. QCA1 gate design [2] **b.** QCA2 gate design [2]

The QCA1 and QCA2 gate input and output relationships are respectively in accordance with formulas 1 and 2.

$$y1 = M(x1, x2, x3) = x1x2 + x2x3 + x1x3$$

$$y2 = M\ (x1, x2, \bar{x3}) = x1x2 + x2\bar{x3} + x1\bar{x3} \quad (1)$$

$$y3 = M\ (\bar{x1}, x2, x3) = \bar{x1}x2 + x2x3 + \bar{x1}x3$$

$$y1 = M\ (x1, x2, x3) = x1x2 + x2x3 + x1x3$$

$$y2 = M\ (x1, x2, \bar{x3}) = x1x2 + x2\bar{x3} + x1\bar{x3} \quad (2)$$

$$y3 = M\ (\bar{x1}, x2, \bar{x3}) = \bar{x1}x2 + x2\bar{x3} + \bar{x1}\bar{x3}$$

In Table 1, four gates of Fredkin and Toffoli, QCA1 and QCA2 have been compared. We see that these two structures are superior to common gateways in reversible circuits for implementation with QCA cells.

Table 1. Comparison between four reversible gates [2]

	Fredkin	Toffoli	QCA1	QCA2
Clock Zones	4	4	2	2
MVs	6	4	3	3
Area	30 * 18	31*18	27*15	27*15
Control cells	6	2	0	0
Normal Cells Non-rotated rotated	185 122 63	167 140 27	146 100 46	146 100 47

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As shown in figure 2, we have reversible gate, that the input of Xn is entered in to it, and we received Yn outputs. If these outputs enter at the reversible gate R means R`, then the result will be that the first inputs of Xn. Then, in figure 3, we have Finman's reversible gate, which, as shown in figure 3b, if one of its inputs is set to zero, it acts like a buffer [4].

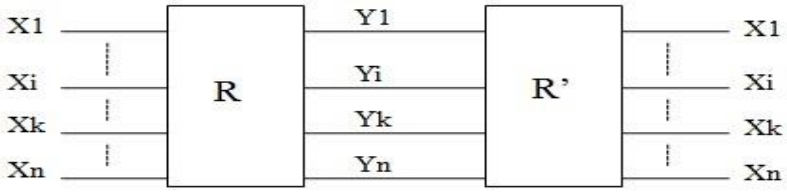

Figure 2. Connecting the two reversible Gates of the R sample and R` is the reverse it [4]

The main challenge in this article is that if we want to Get multiple outputs from the reversible gate, then the operation of the circuit will have an error. The solution is using each gate alongside its reverse and then getting help from the designed buffer to get multiple outputs. In this way, in the reversible gate output, we have that first input and can be applied to the circuit and at the same time we can have an instance of it to detect the error. You can use this method for each line.

As shown in Figure 3, we can design IQCA2 and IQCA1 gates for QCA1 and QCA2 gates as their reverse, and all circuits designed with them by helping the Presented buffer we can detection an error.

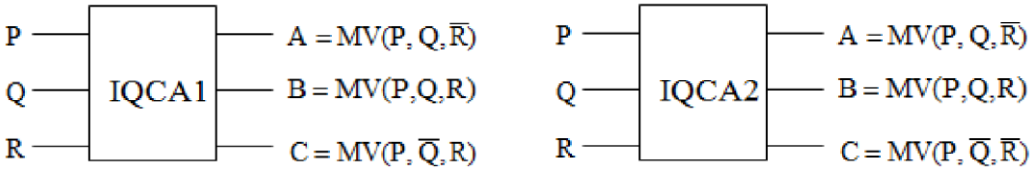

Figure 3. a. QCA 1 Reversible Gate [4] **b.** Reversible Gate QCA [4]

3. Reversible multiplexer

With regard to the reversible gate of QCA1 and the input and output relationships of this gate, as shown in relationship 1 and 2 [2] and reversible circuits [4] and by using XOR gate, can be design multiplexer 2*1 of revisable to the schematic of Figure 4 provided [5]. The design of this multiplexer simulated using the QCA Designer software, is shown in Figure 5. And the correct table of proposed reversible multiplexer, is shown in Table 2.

And by using three multiplexers 2*1, can design a multiplexer 4*1according to Figure 6. wich in that A1 and A2 will be address, and I0, I1, I2, and I3 will be selected as inputs, and Y will be selected as multiplexer output. And the correct table of proposed reversible multiplexer, is shown in Table 3.

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Table 2. The correct table of reversible multiplexer 2*1

A	R
0	B
1	C

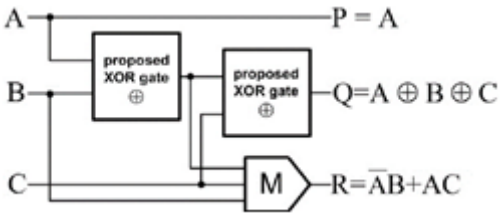

Figure 4. Schematic of reversible multiplexer 2*1

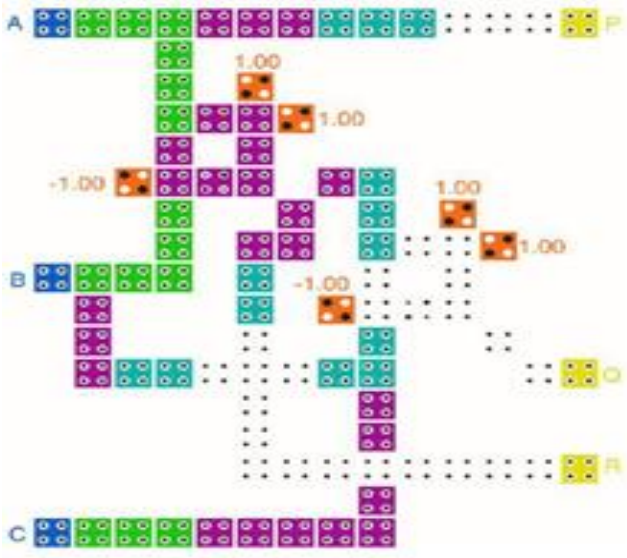

Figure 5. QCA layout of full reversible multiplexer 2*1 circuit

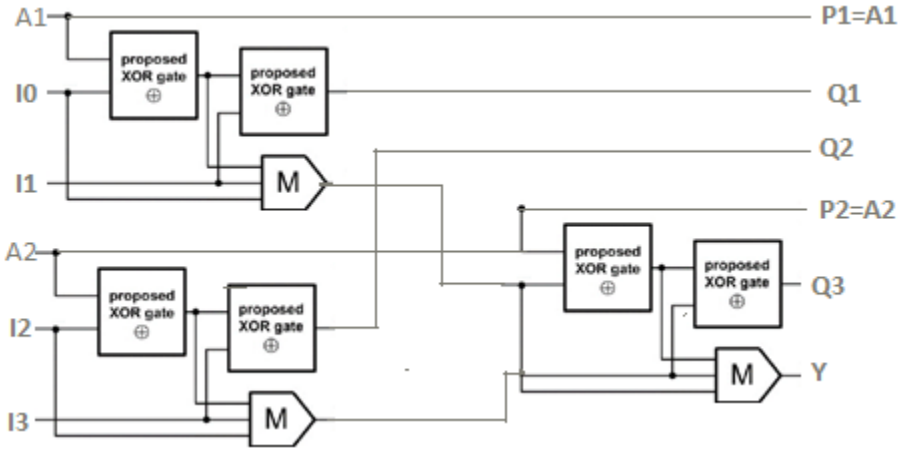

Figure 6. Schematic of proposed reversible multiplexer 4*1

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Table 2. The correct table of reversible multiplexer 4*1

A1	A0	Y(OUT)
0	0	I0
0	1	I1
1	0	I2
1	1	I3

4. Conclusion

Circuit design using reversible gates causes the circuit to not lose energy, because it retrieves lost energy and prevents bit error by using error tolerance mechanisms. Given the growing importance of reducing energy consumption, the QCA technology reversible logic concept is a new issue, which reduces power dissipation in circuits.
In this paper, by using three multiplexers 2*1, design a reversible multiplexer 4*1 was designed, and this multiplexer is simulated the QCA Designer software. Therefore, according to its reversibility, power consumption was reduced, and by error tolerance mechanisms, a bit error is prevented.

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